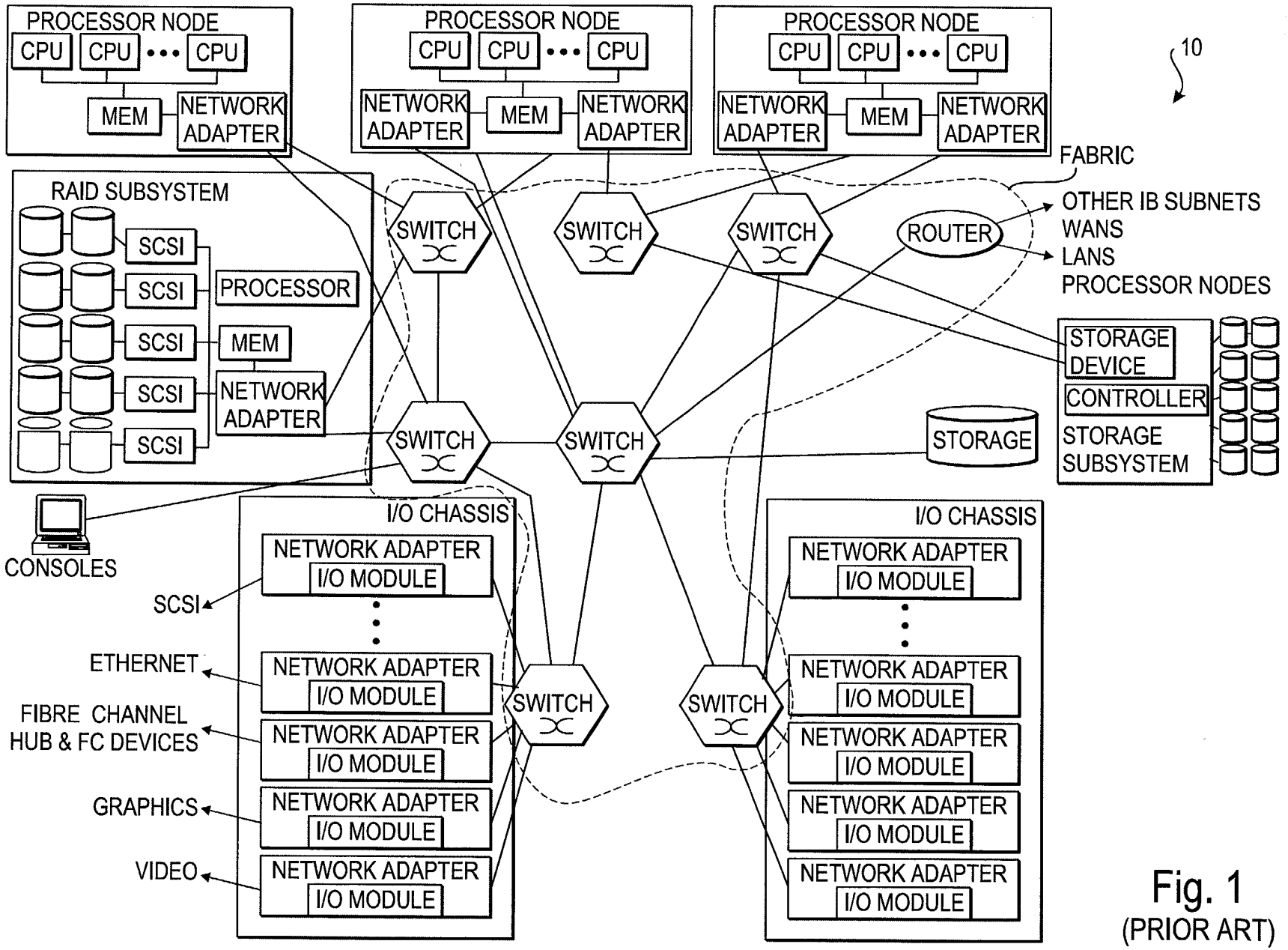


Fig. 1
(PRIOR ART)

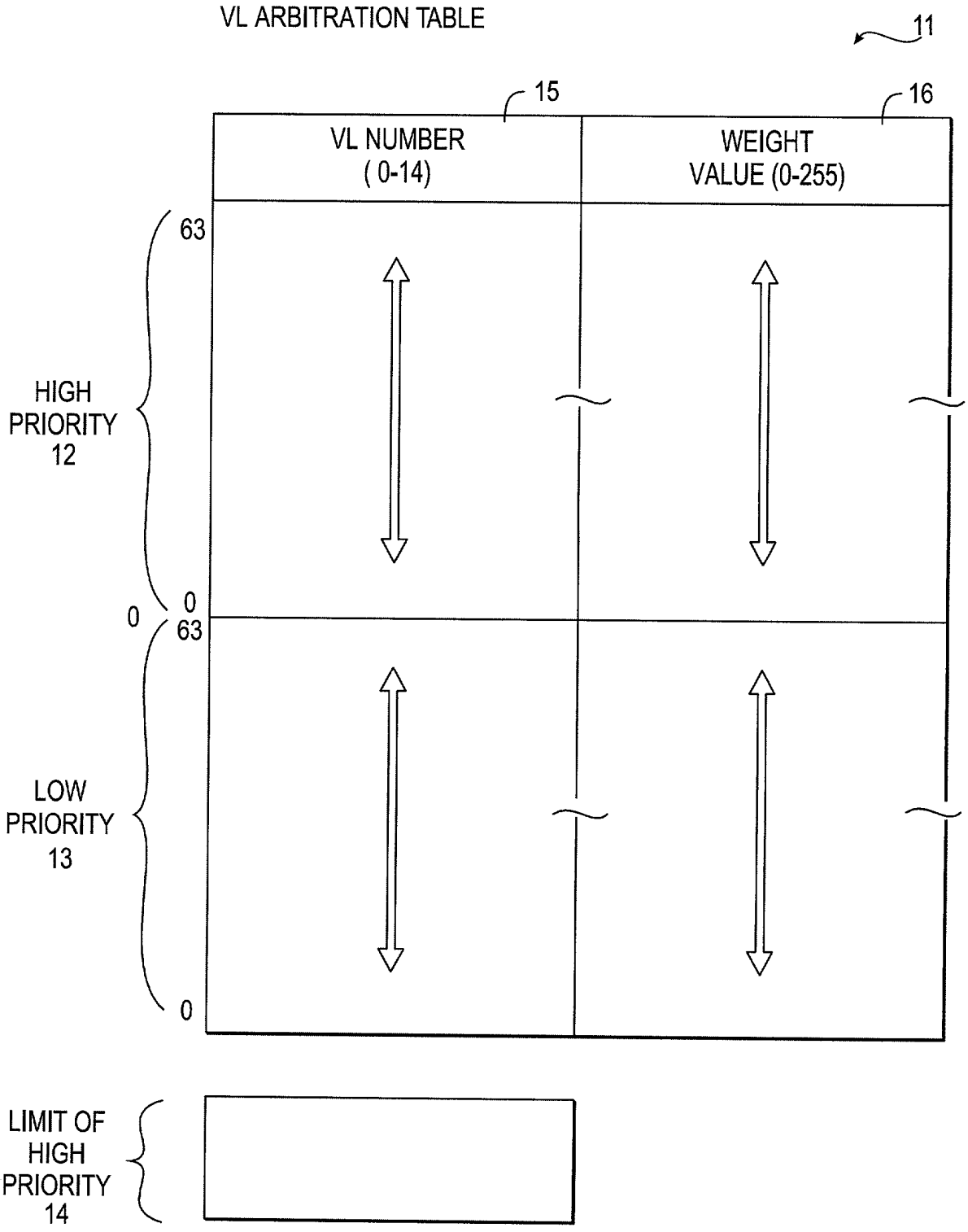
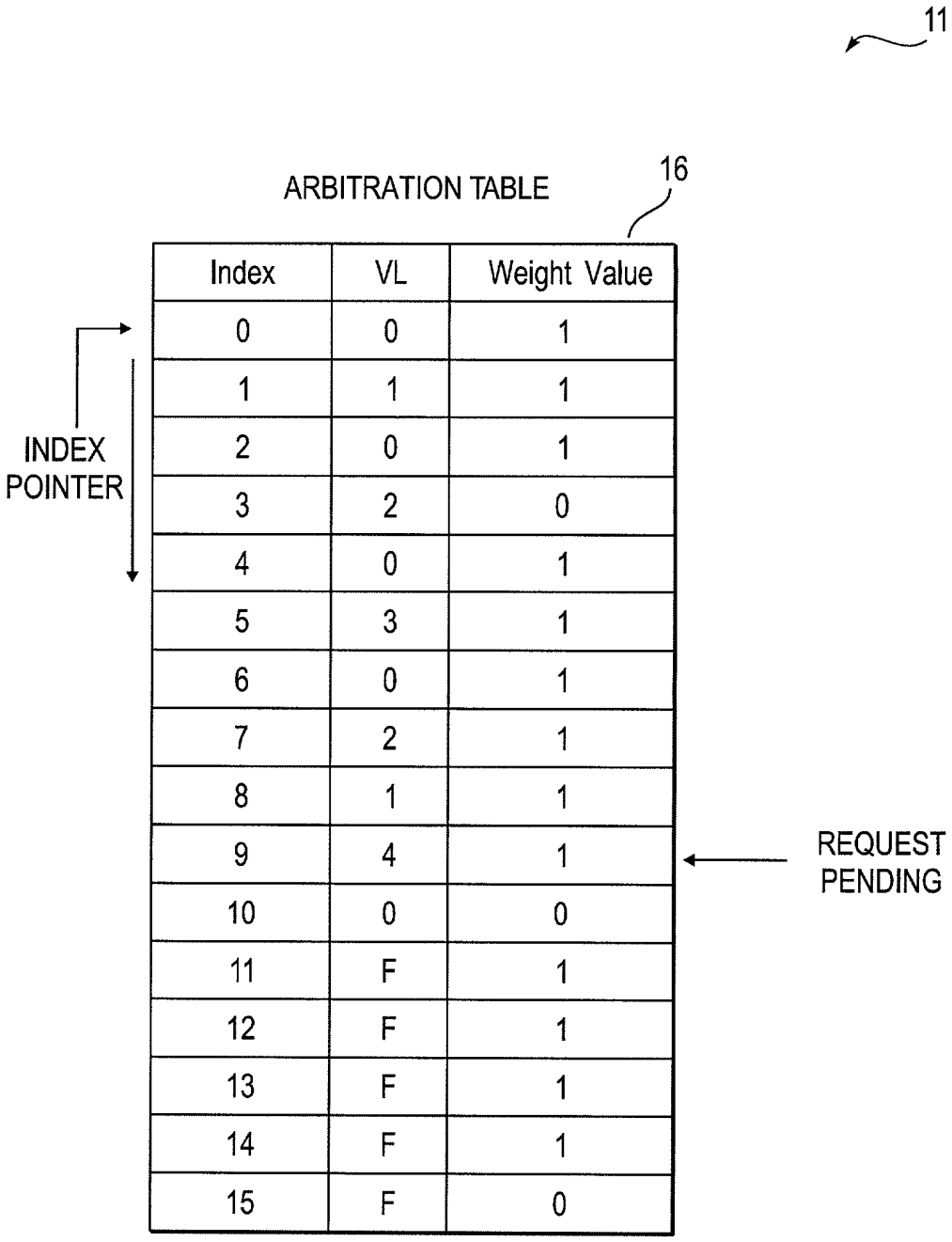


Fig. 2A
(PRIOR ART)



Index	VL	Weight Value
0	0	1
1	1	1
2	0	1
3	2	0
4	0	1
5	3	1
6	0	1
7	2	1
8	1	1
9	4	1
10	0	0
11	F	1
12	F	1
13	F	1
14	F	1
15	F	0

Fig. 2B
(PRIOR ART)

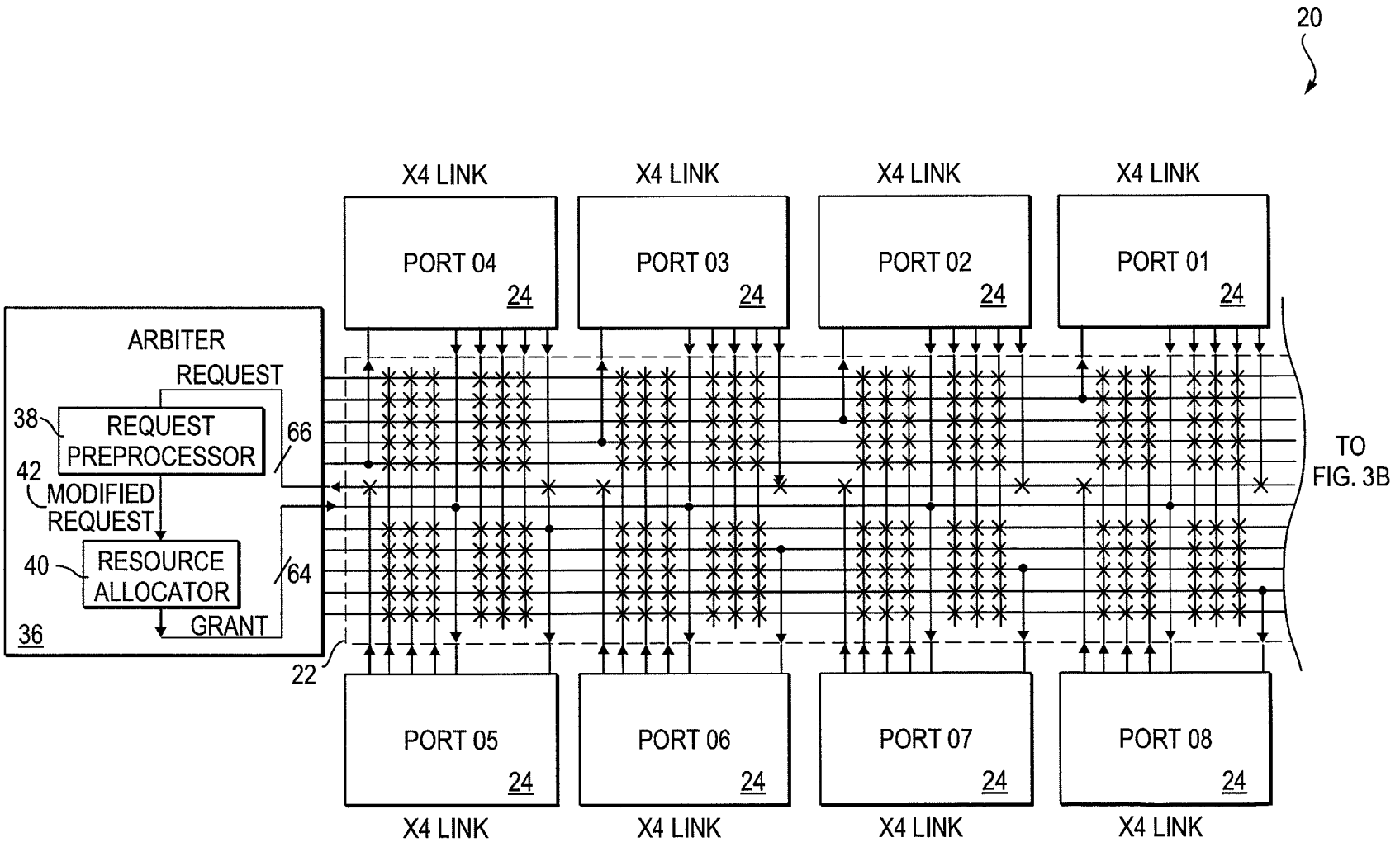

20
X4 LINK
X4 LINK
X4 LINK
X4 LINK
PORT 04
24
PORT 03
24
PORT 02
24
PORT 01
24
ARBITER
REQUEST
38
REQUEST
PREPROCESSOR
66
42
MODIFIED
REQUEST
40
RESOURCE
ALLOCATOR
64
GRANT
36
22
TO
FIG. 3B
PORT 05
24
PORT 06
24
PORT 07
24
PORT 08
24
X4 LINK
X4 LINK
X4 LINK
X4 LINK

Fig. 3A

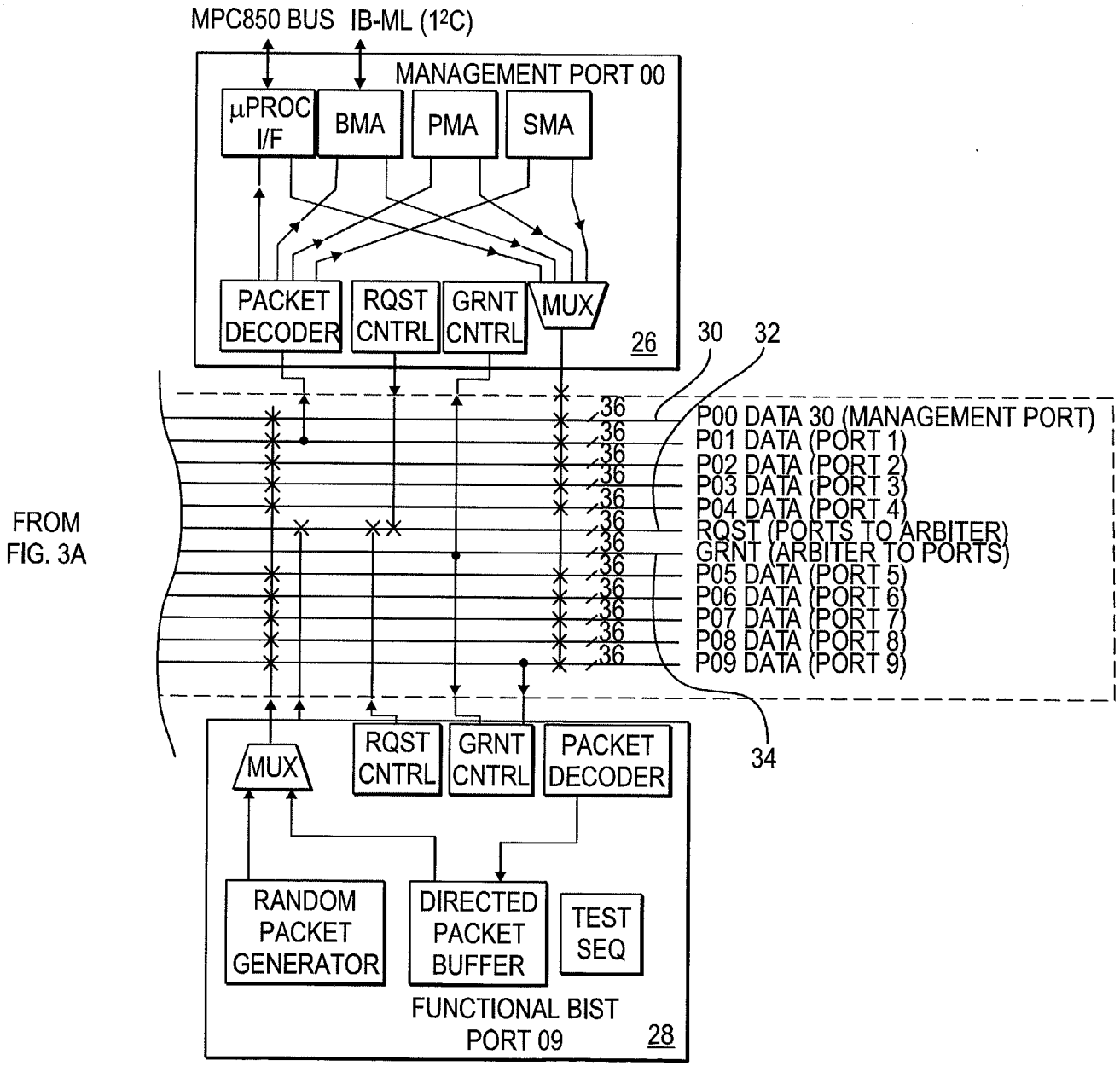

MPC850 BUS
IB-ML (I²C)
MANAGEMENT PORT 00
µPROC I/F
BMA
PMA
SMA
PACKET DECODER
RQST CNTRL
GRNT CNTRL
MUX
26
30
32
FROM FIG. 3A
36
P00 DATA 30 (MANAGEMENT PORT)
P01 DATA (PORT 1)
P02 DATA (PORT 2)
P03 DATA (PORT 3)
P04 DATA (PORT 4)
RQST (PORTS TO ARBITER)
GRNT (ARBITER TO PORTS)
P05 DATA (PORT 5)
P06 DATA (PORT 6)
P07 DATA (PORT 7)
P08 DATA (PORT 8)
P09 DATA (PORT 9)
34
MUX
RQST CNTRL
GRNT CNTRL
PACKET DECODER
RANDOM PACKET GENERATOR
DIRECTED PACKET BUFFER
TEST SEQ
FUNCTIONAL BIST PORT 09
28

Fig. 3B

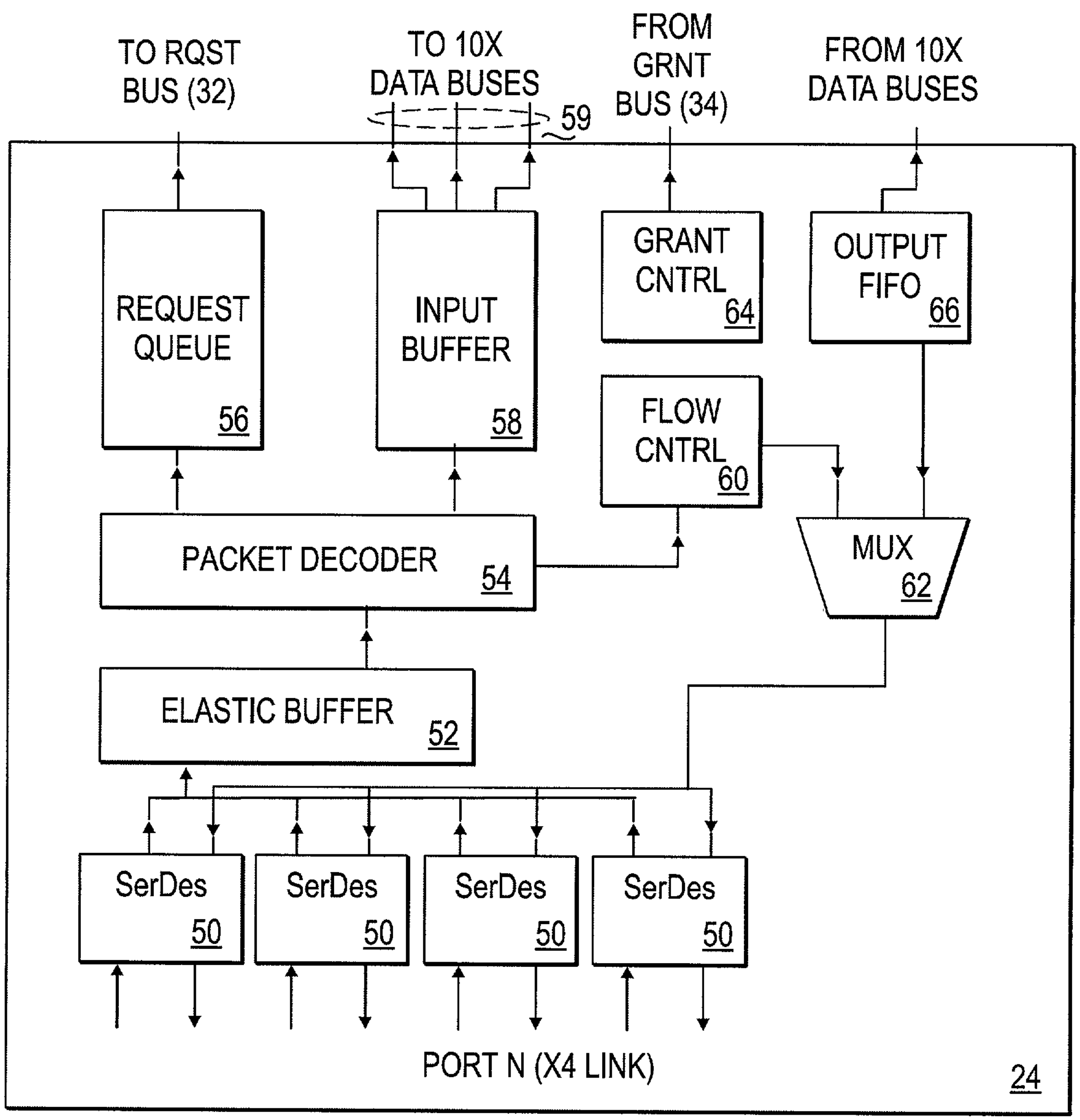

TO RQST BUS (32)
TO 10X DATA BUSES
59
FROM GRNT BUS (34)
FROM 10X DATA BUSES
REQUEST QUEUE 56
INPUT BUFFER 58
GRANT CNTRL 64
OUTPUT FIFO 66
FLOW CNTRL 60
PACKET DECODER 54
MUX 62
ELASTIC BUFFER 52
SerDes 50
SerDes 50
SerDes 50
SerDes 50
PORT N (X4 LINK)
24

Fig. 4

DESTINATION ROUTING REQUEST 70

REQUEST EXTENSION (2 BIT) 96	PARTITION KEY (16 BIT) 92	DESTINATION ADDRESS (16 BIT) 90	SERVICE LEVEL (4 BIT) 94	PACKET LENGTH (11 BIT) 86	REQUEST ID (10 BIT) 84	INPUT PORT (5 BIT) 82	REQUEST CODE (2 BIT) 80

DIRECT ROUTING REQUEST 72

REQUEST EXTENSION (2 BIT) 76	RESERVED (27 BIT)	OUTPUT PORT (5 BIT) 88	VIRTUAL LANE (4 BIT) 102	PACKET LENGTH (11 BIT) 86	REQUEST ID (10 BIT) 84	INPUT PORT (5 BIT) 82	REQUEST CODE (2 BIT) 80

CREDIT UPDATE REQUEST 74

PORT STATUS (2BIT) 98	RESERVED (27 BIT)	OUTPUT PORT (5 BIT) 88	VIRTUAL LANE (4 BIT) 102	FLOW CONTROL CREDIT LIMIT (FCCL) (12 BIT) 104	RESERVED (9 BIT)	INPUT PORT (5 BIT) 82	REQUEST CODE (2 BIT) 80

Fig. 5

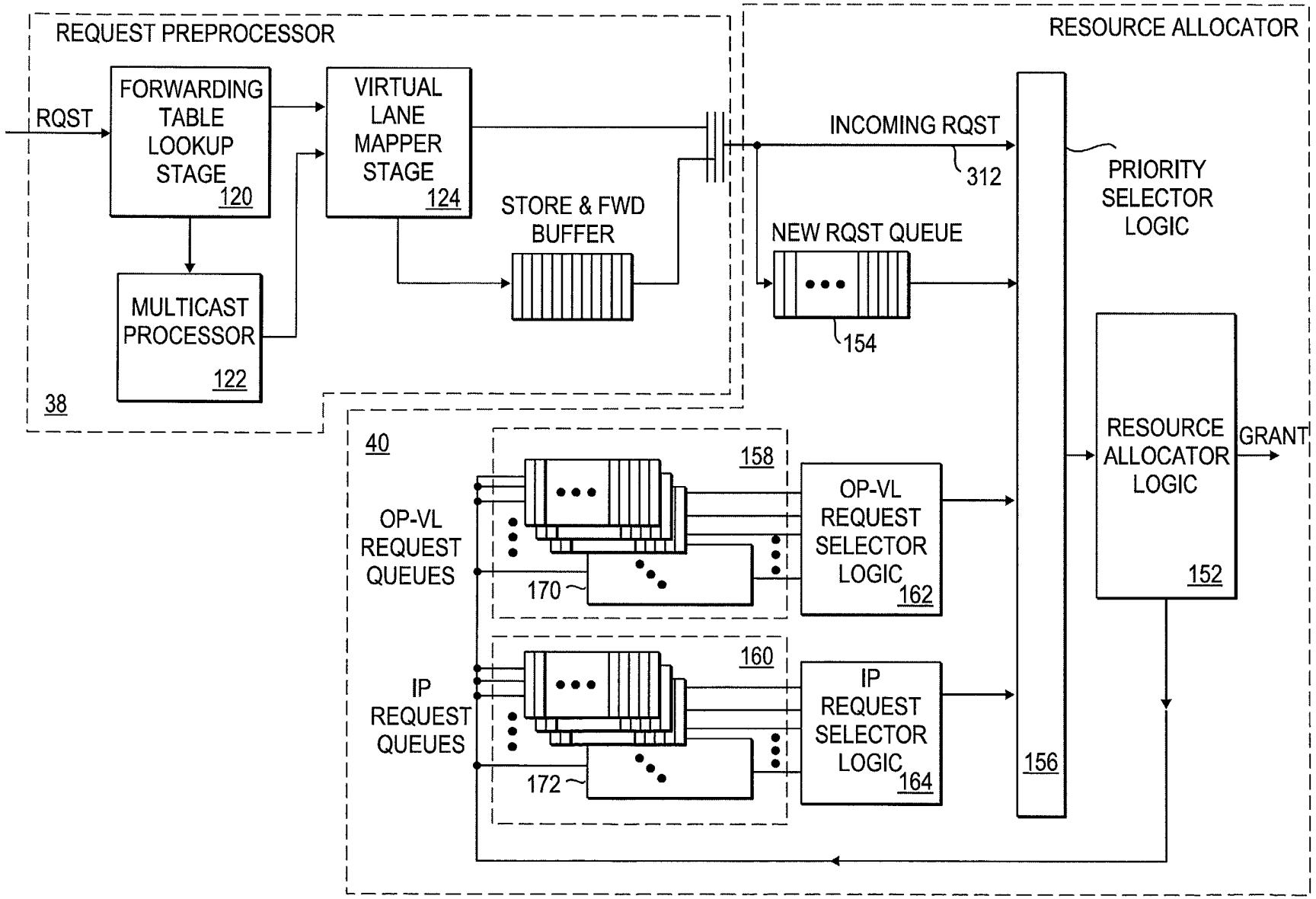

REQUEST PREPROCESSOR
RESOURCE ALLOCATOR
RQST
FORWARDING TABLE LOOKUP STAGE
120
VIRTUAL LANE MAPPER STAGE
124
STORE & FWD BUFFER
MULTICAST PROCESSOR
122
38
INCOMING RQST
312
NEW RQST QUEUE
154
PRIORITY SELECTOR LOGIC
40
158
OP-VL REQUEST QUEUES
170
OP-VL REQUEST SELECTOR LOGIC
162
160
IP REQUEST QUEUES
172
IP REQUEST SELECTOR LOGIC
164
156
RESOURCE ALLOCATOR LOGIC
152
GRANT

Fig. 6

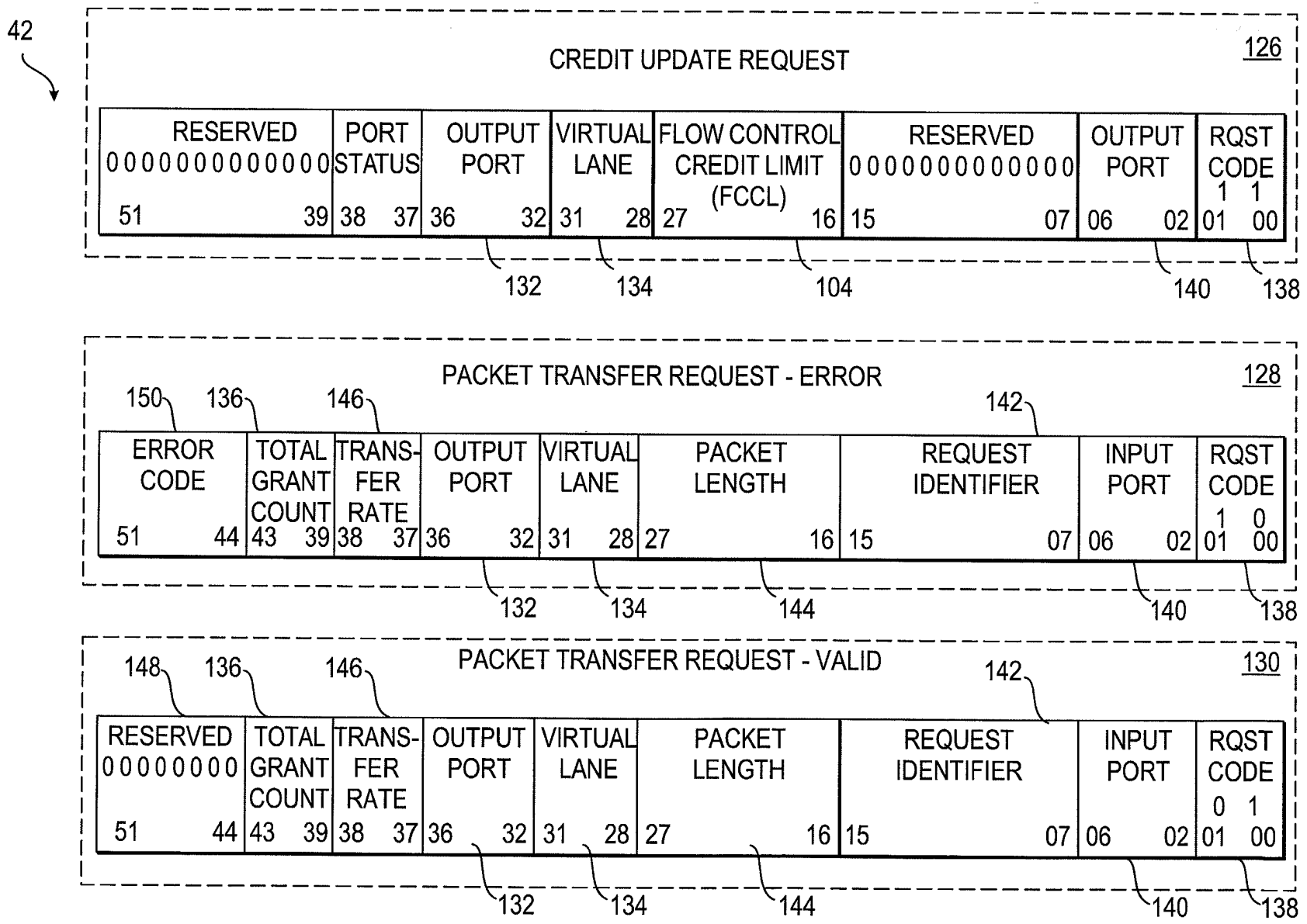
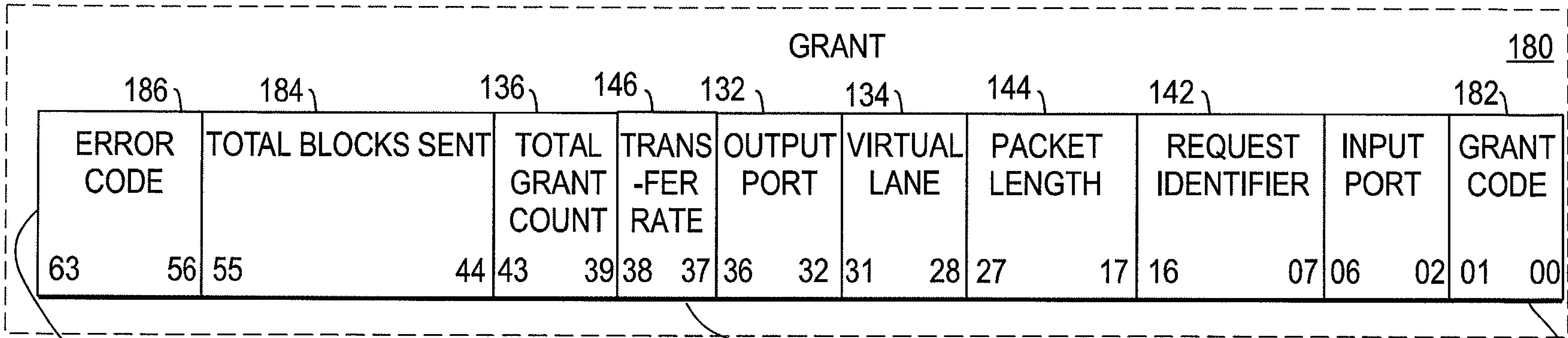

42
CREDIT UPDATE REQUEST
126
RESERVED
000000000000
51 39
PORT STATUS
38 37
OUTPUT PORT
36 32
VIRTUAL LANE
31 28
FLOW CONTROL CREDIT LIMIT (FCCL)
27 16
RESERVED
0000000000000
15 07
OUTPUT PORT
06 02
RQST CODE
1 1
01 00
132
134
104
140
138
PACKET TRANSFER REQUEST - ERROR
128
150
136
146
142
ERROR CODE
51 44
TOTAL GRANT COUNT
43 39
TRANS-FER RATE
38 37
OUTPUT PORT
36 32
VIRTUAL LANE
31 28
PACKET LENGTH
27 16
REQUEST IDENTIFIER
15 07
INPUT PORT
06 02
RQST CODE
1 0
01 00
132
134
144
140
138
PACKET TRANSFER REQUEST - VALID
130
148
136
146
142
RESERVED
00000000
51 44
TOTAL GRANT COUNT
43 39
TRANS-FER RATE
38 37
OUTPUT PORT
36 32
VIRTUAL LANE
31 28
PACKET LENGTH
27 16
REQUEST IDENTIFIER
15 07
INPUT PORT
06 02
RQST CODE
0 1
01 00
132
134
144
140
138

Fig. 7



ERROR CODE

VALUE	MEANING
000 00000	NO ERROR
0X0 00001	UNICAST DLID OUT-OF-RANGE
0X0 00010	UNICAST FORWARDING TALE ENTRY NOT VALID OR DEFAULT MULTICAST PORT REGISTERS NOT VALID
0X0 00011	OUTPUT PORT NOT VALID FOR MGMT PORT DIRECTED-ROUTE PACKET
0X1 XXXX1	(OUTPUT PORT = INPUT PORT) & (PORT = 0)
0X1 XXX1X	SL-TO-VL MAP TABLE ENTRY NOT VALID
0X1 XX1XX	PACKET LARGER THAN NEIGHBOR MTU
0X1 10XXX	RAW PACKET NOT VALID FOR OUTPUT PORT
0X1 11XXX	P-KEY NOT VALID FOR OUTPUT PORT
01X XXXXX	P-KEY NOT VALID FOR INPUT PORT
111 11101	OUTPUT PORT OFFLINE
111 11110	HEAD-OF-QUEUE LIFETIME TIMEOUT
111 11111	SWITCH LIFETIME TIMEOUT

TRANSFER RATE

VALUE	MEANING
00	1 CYCLE PER WORD
01	4 CYCLES PER WORD
10	3 CYCLES PER WORD (RESERVED)
11	12 CYCLES PER WORD (RESERVED)

GRANT CODE

VALUE	MEANING
00	NULL
01	VALID
10	ERROR
11	RESERVED

Fig. 8

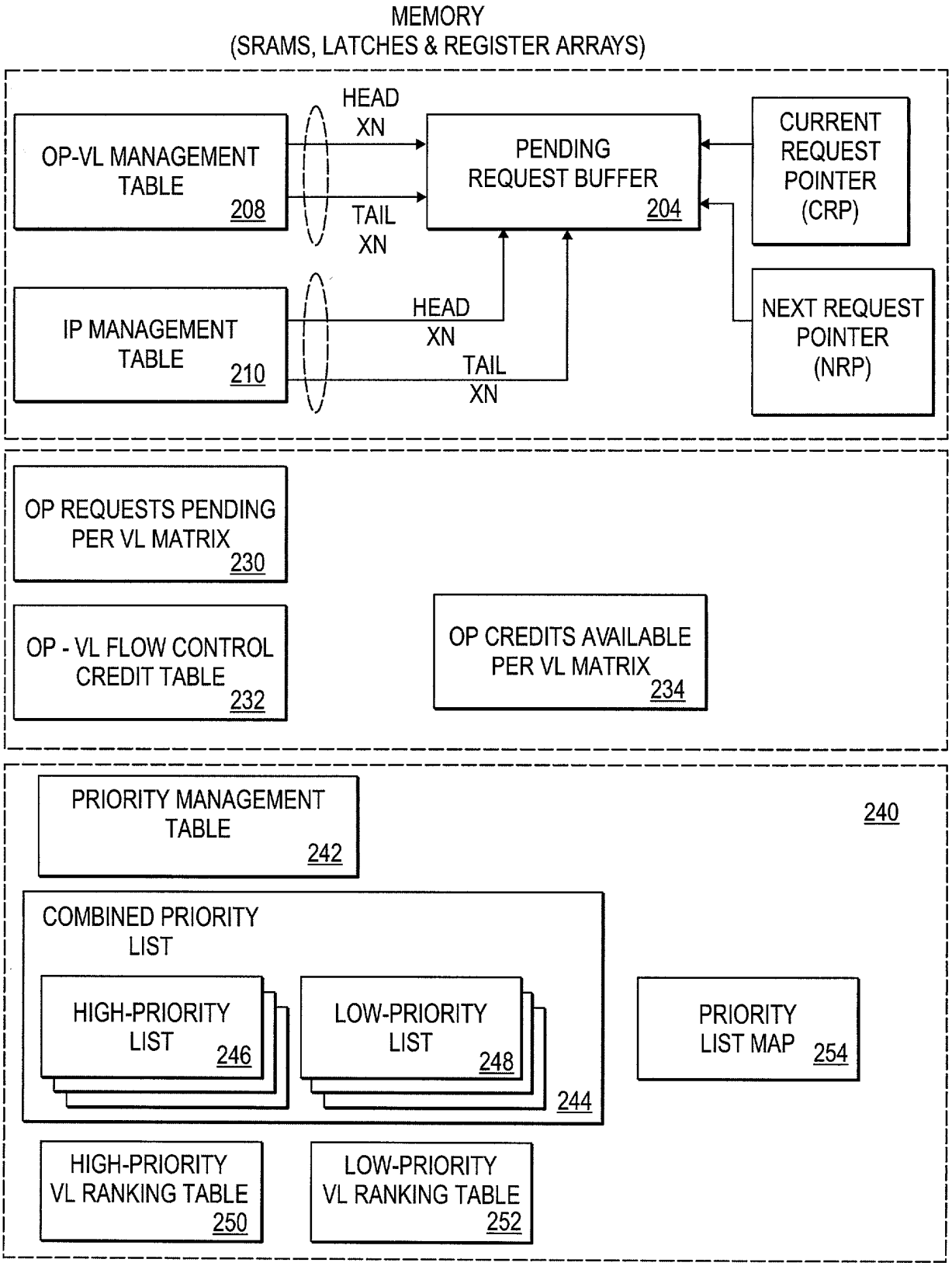


Fig. 9

Combined Priority List Address Map

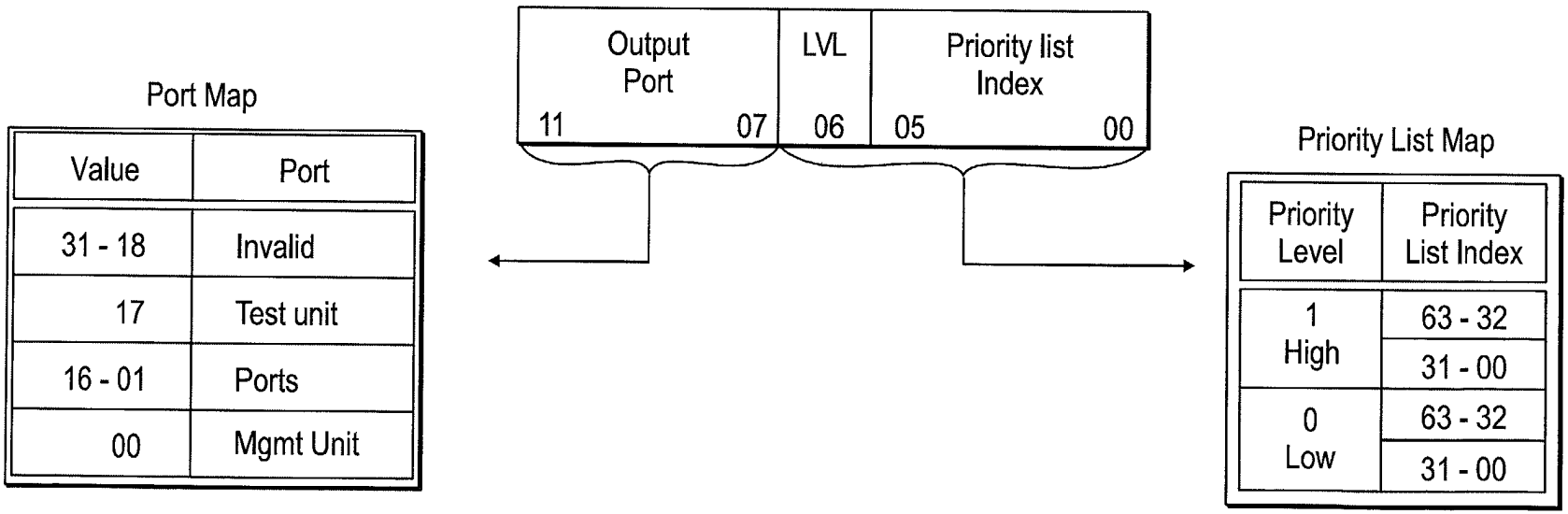
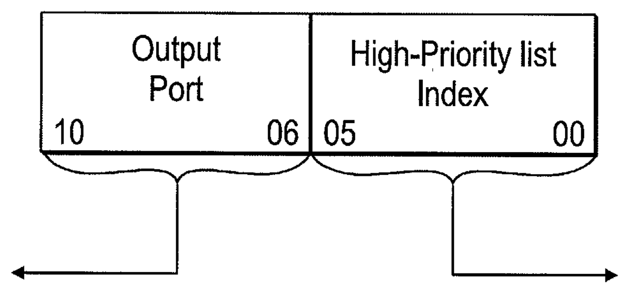


Fig. 10A

High-Priority VL Ranking Table - Address Map

Port Map

Value	Port
31 - 18	Invalid
17	Test unit
16 - 01	Ports
00	Mgmt Unit



High-Priority List Map

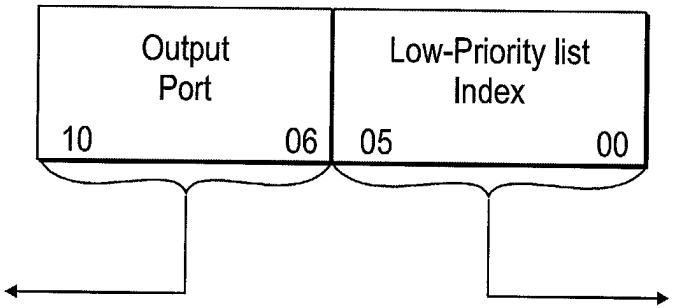
High-Priority List Index
63 - 32
31 - 00

Fig. 10B

Low-Priority VL Ranking Table - Address Map

Port Map

Value	Port
31 - 18	Invalid
17	Test unit
16 - 01	Ports
00	Mgmt Unit



Low-Priority List Map

Low-Priority List Index
63 - 32
31 - 00

Fig. 10C

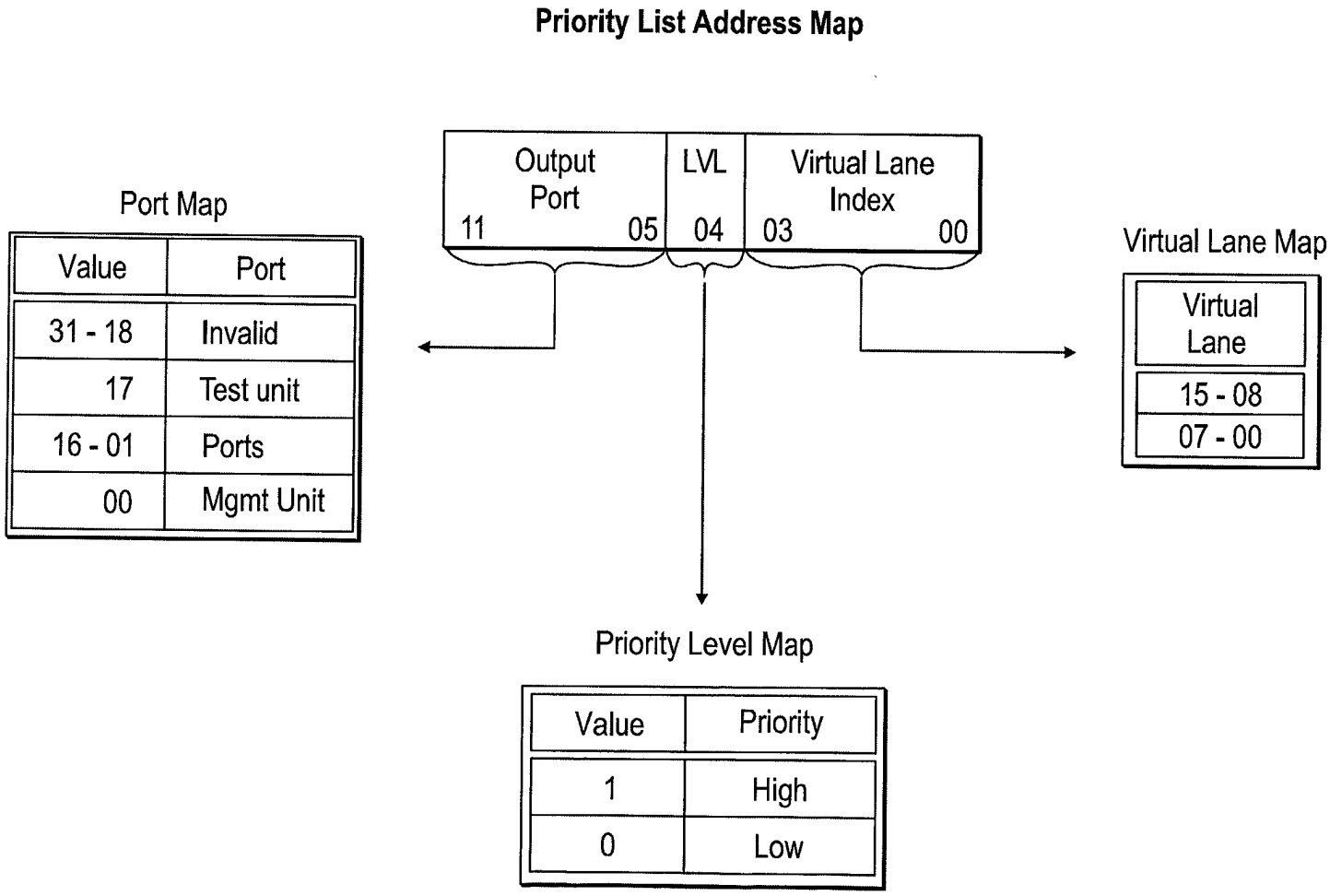

Priority List Address Map
Output Port
11
05
LVL
04
Virtual Lane Index
03
00
Port Map
Value
Port
31 - 18
Invalid
17
Test unit
16 - 01
Ports
00
Mgmt Unit
Virtual Lane Map
Virtual Lane
15 - 08
07 - 00
Priority Level Map
Value
Priority
1
High
0
Low

Fig. 10D

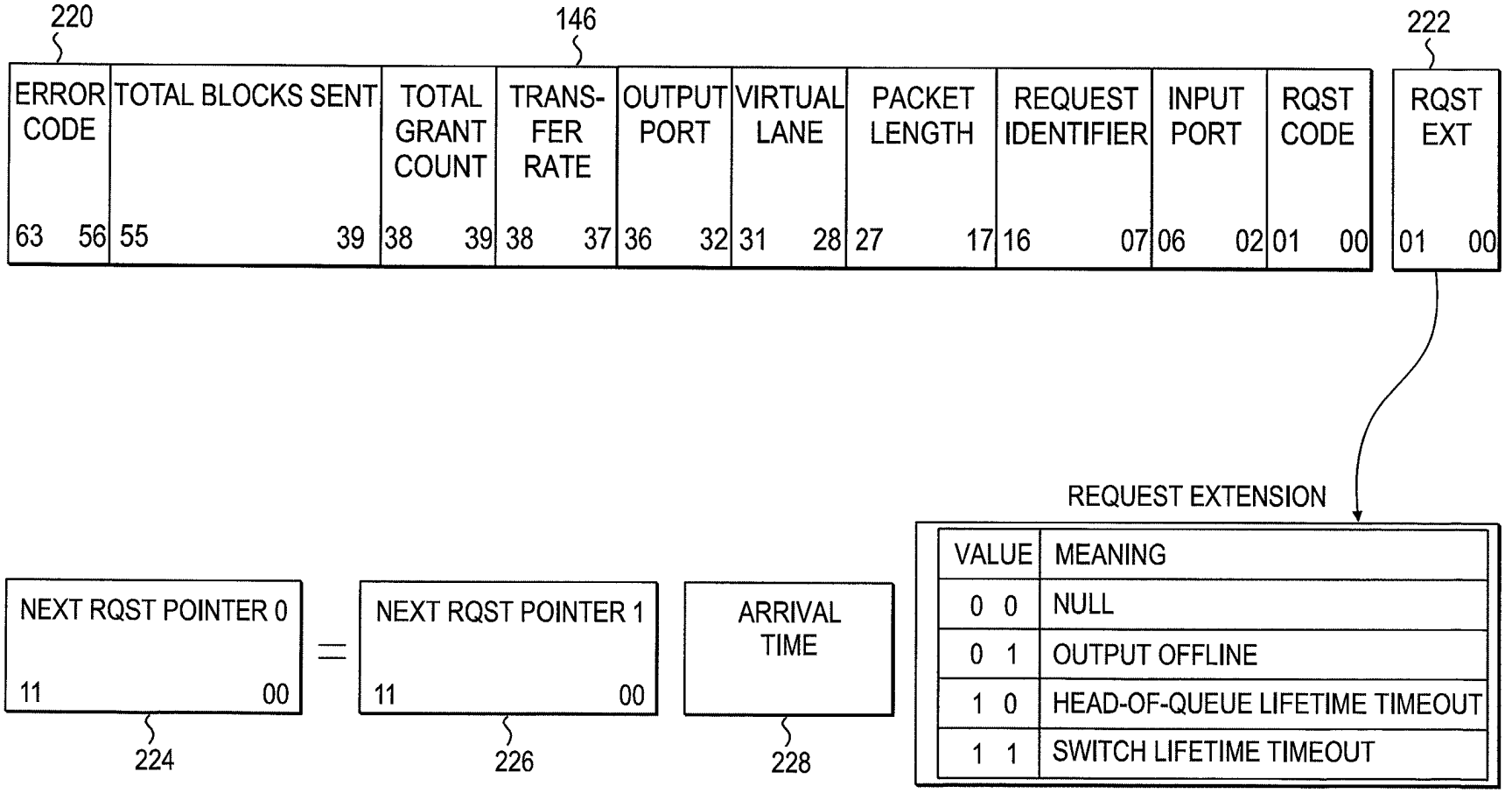

220
146
222
ERROR CODE
63 56
TOTAL BLOCKS SENT
55 39
TOTAL GRANT COUNT
38 39
TRANS-FER RATE
38 37
OUTPUT PORT
36 32
VIRTUAL LANE
31 28
PACKET LENGTH
27 17
REQUEST IDENTIFIER
16 07
INPUT PORT
06 02
RQST CODE
01 00
RQST EXT
01 00
REQUEST EXTENSION
VALUE
MEANING
0 0
NULL
0 1
OUTPUT OFFLINE
1 0
HEAD-OF-QUEUE LIFETIME TIMEOUT
1 1
SWITCH LIFETIME TIMEOUT
NEXT RQST POINTER 0
11 00
=
NEXT RQST POINTER 1
11 00
ARRIVAL TIME
224
226
228

Fig. 11

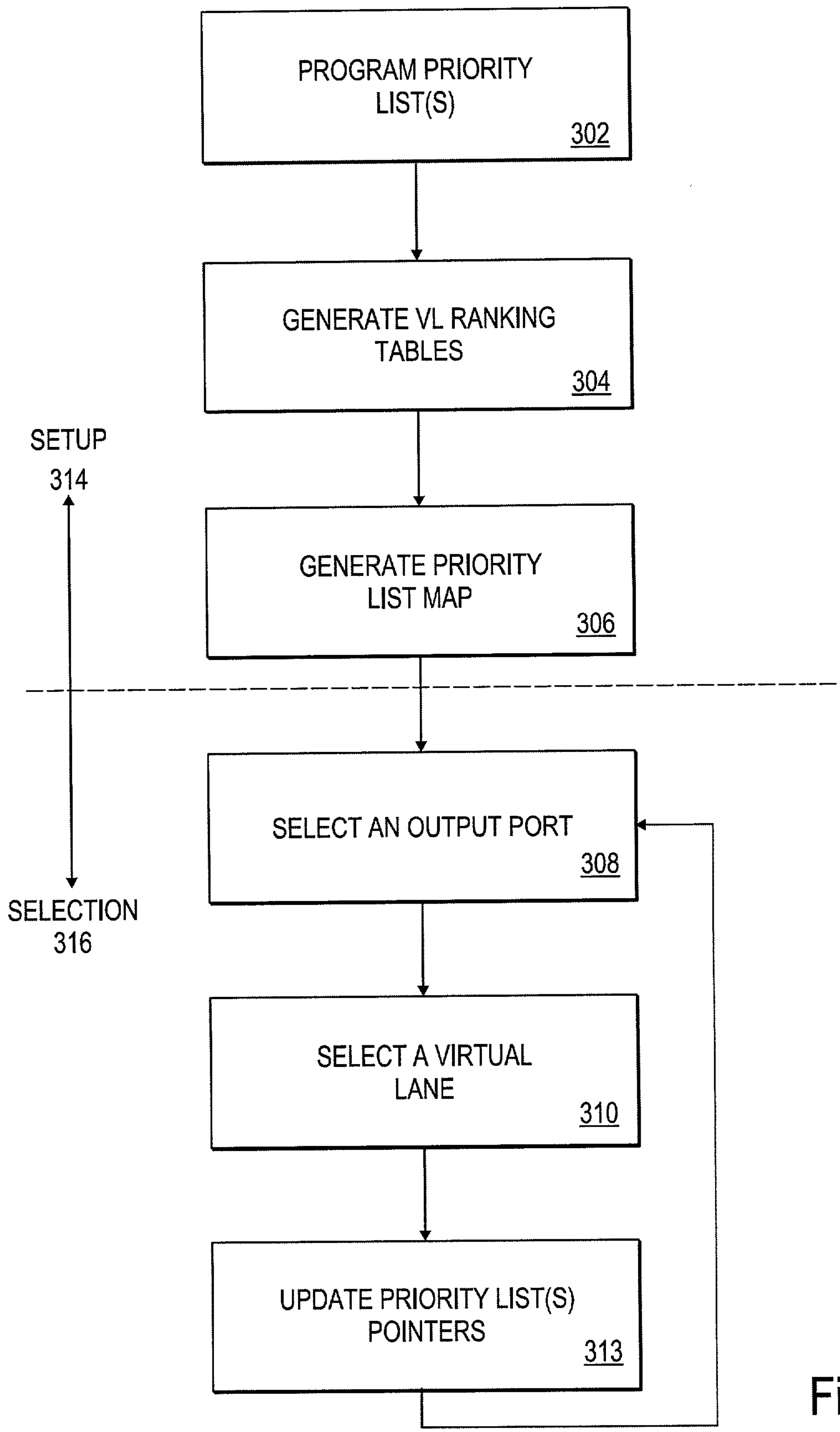

PROGRAM PRIORITY LIST(S)
302
GENERATE VL RANKING TABLES
304
GENERATE PRIORITY LIST MAP
306
SETUP
314
SELECTION
316
SELECT AN OUTPUT PORT
308
SELECT A VIRTUAL LANE
310
UPDATE PRIORITY LIST(S) POINTERS
313

Fig. 12

COMBINED PRIORITY LIST 244

Index	VL	Weight
0	0	1
1	1	1
2	0	1
3	2	0
4	0	1
5	3	1
6	0	1
7	2	1
8	1	1
9	4	1
10	0	0
11	F	1
12	F	1
13	F	1
14	F	1
15	F	0

318

HIGH-PRIORITY VIRTUAL LANE RANKING TABLE 250

Index	RANKING VECTOR(Hex)
0	0132_4FFF_FFFF_FFFF
1	1032_4FFF_FFFF_FFFF
2	0321_4FFF_FFFF_FFFF
3	0321_4FFF_FFFF_FFFF
4	0321_4FFF_FFFF_FFFF
5	3021_4FFF_FFFF_FFFF
6	0214_3FFF_FFFF_FFFF
7	2140_3FFF_FFFF_FFFF
8	1403_2FFF_FFFF_FFFF
9	4013_2FFF_FFFF_FFFF
10	0132_4FFF_FFFF_FFFF
11	0132_4FFF_FFFF_FFFF
12	0132_4FFF_FFFF_FFFF
13	0132_4FFF_FFFF_FFFF
14	0132_4FFF_FFFF_FFFF
15	0132_4FFF_FFFF_FFFF

251

COMBINED PRIORITY LIST 244

Index	VL	Weight
0	0	1
1	1	1
2	0	1
3	2	0
4	0	1
5	3	1
6	0	1
7	2	1
8	1	1
9	4	1
10	0	0
11	F	1
12	F	1
13	F	1
14	F	1
15	F	0

PRIORITY LIST MAP 254

Index (same as VL)	List Map (Binary)
0	0000_0000_0101_0101
1	0000_0001_0000_0010
2	0000_0000_1000_0000
3	0000_0000_0010_0000
4	0000_0010_0000_0000
5	0000_0000_0000_0000
6	0000_0000_0000_0000
7	0000_0000_0000_0000

255

Fig. 13

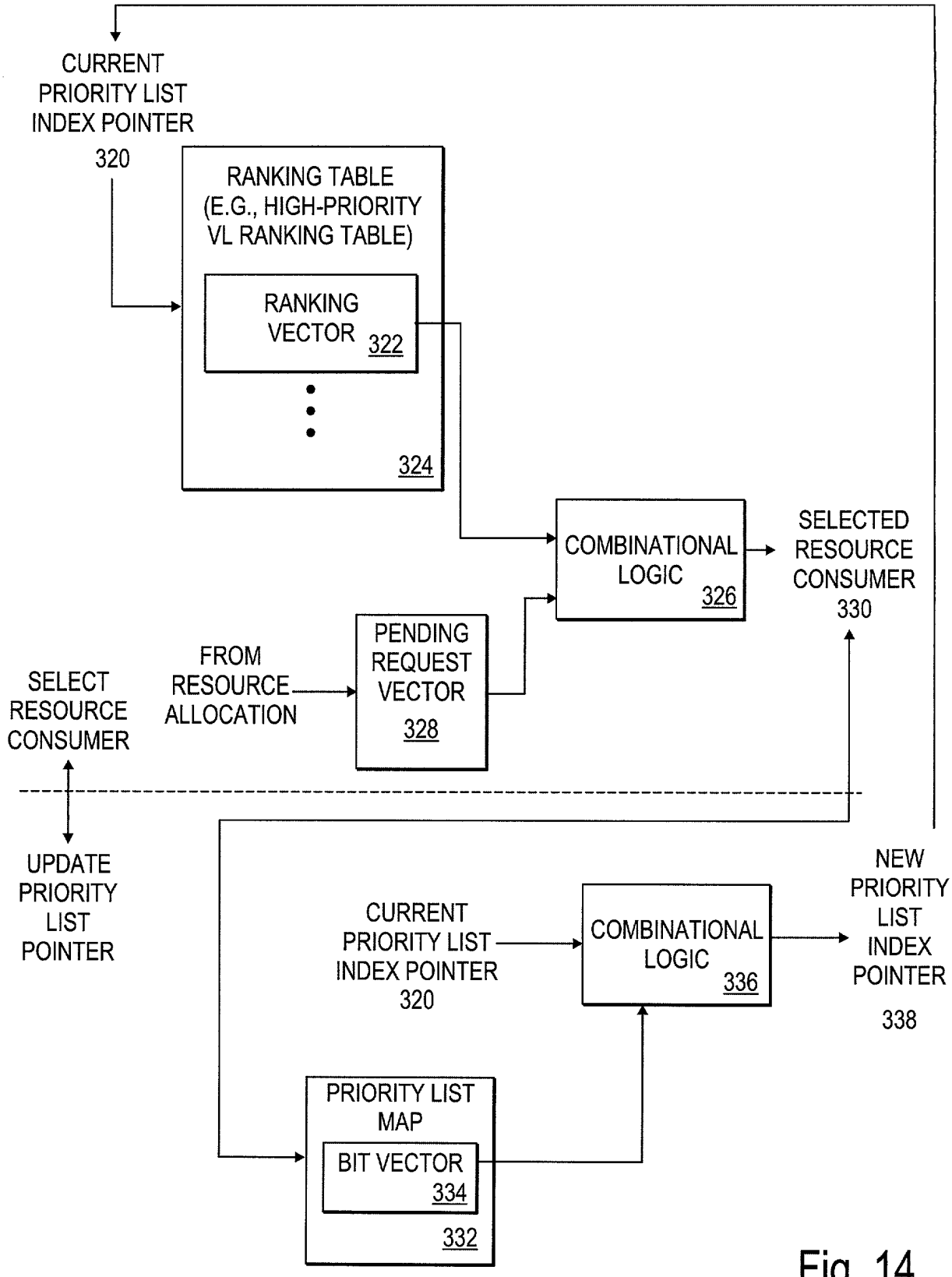

CURRENT
PRIORITY LIST
INDEX POINTER
320
RANKING TABLE
(E.G., HIGH-PRIORITY
VL RANKING TABLE)
RANKING
VECTOR
322
324
COMBINATIONAL
LOGIC
326
SELECTED
RESOURCE
CONSUMER
330
PENDING
REQUEST
VECTOR
328
FROM
RESOURCE
ALLOCATION
SELECT
RESOURCE
CONSUMER
UPDATE
PRIORITY
LIST
POINTER
CURRENT
PRIORITY LIST
INDEX POINTER
320
COMBINATIONAL
LOGIC
336
NEW
PRIORITY
LIST
INDEX
POINTER
338
PRIORITY LIST
MAP
BIT VECTOR
334
332

Fig. 14

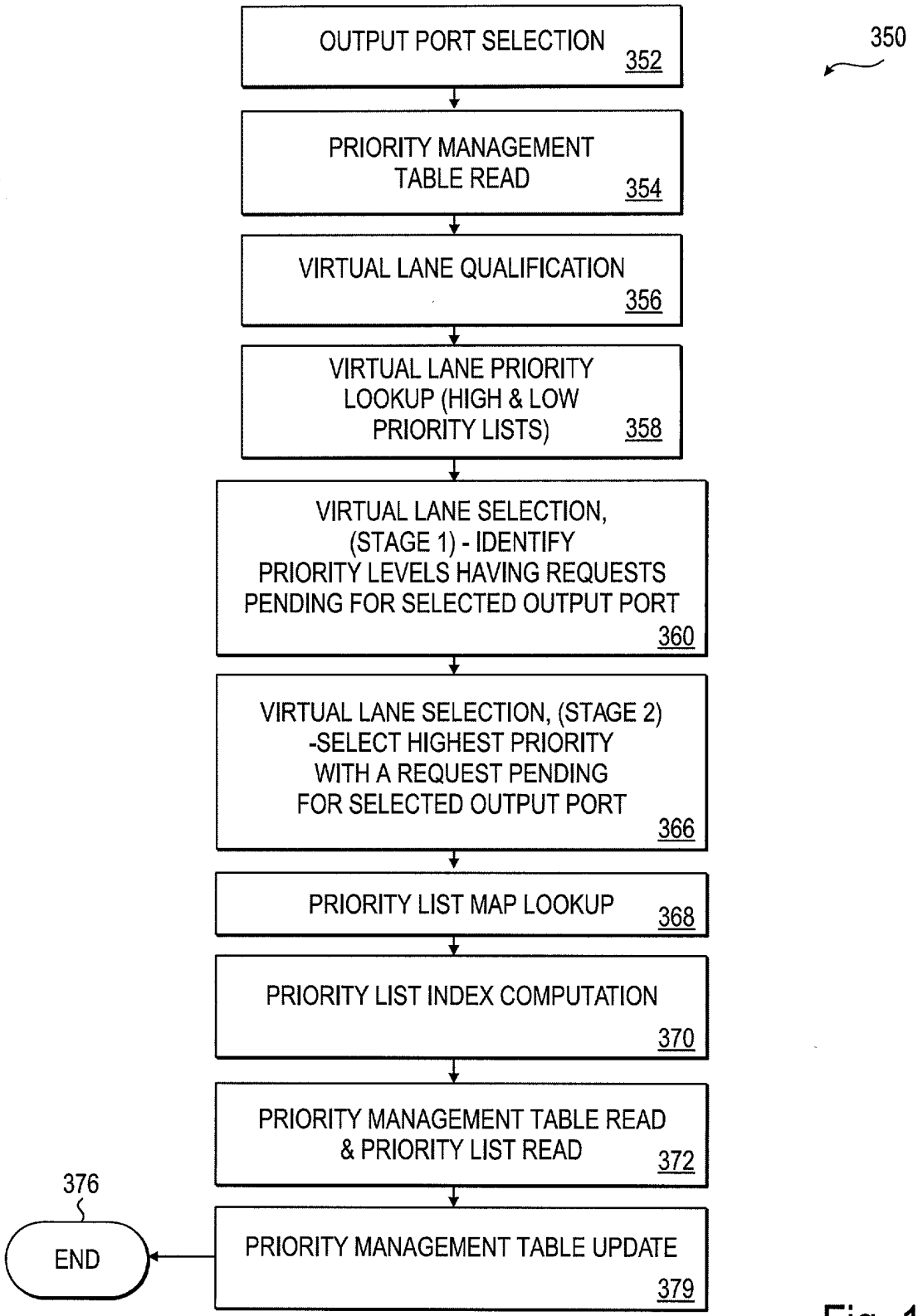

OUTPUT PORT SELECTION 352
350
PRIORITY MANAGEMENT TABLE READ 354
VIRTUAL LANE QUALIFICATION 356
VIRTUAL LANE PRIORITY LOOKUP (HIGH & LOW PRIORITY LISTS) 358
VIRTUAL LANE SELECTION, (STAGE 1) - IDENTIFY PRIORITY LEVELS HAVING REQUESTS PENDING FOR SELECTED OUTPUT PORT 360
VIRTUAL LANE SELECTION, (STAGE 2) -SELECT HIGHEST PRIORITY WITH A REQUEST PENDING FOR SELECTED OUTPUT PORT 366
PRIORITY LIST MAP LOOKUP 368
PRIORITY LIST INDEX COMPUTATION 370
PRIORITY MANAGEMENT TABLE READ & PRIORITY LIST READ 372
376
END
PRIORITY MANAGEMENT TABLE UPDATE 379

Fig. 15

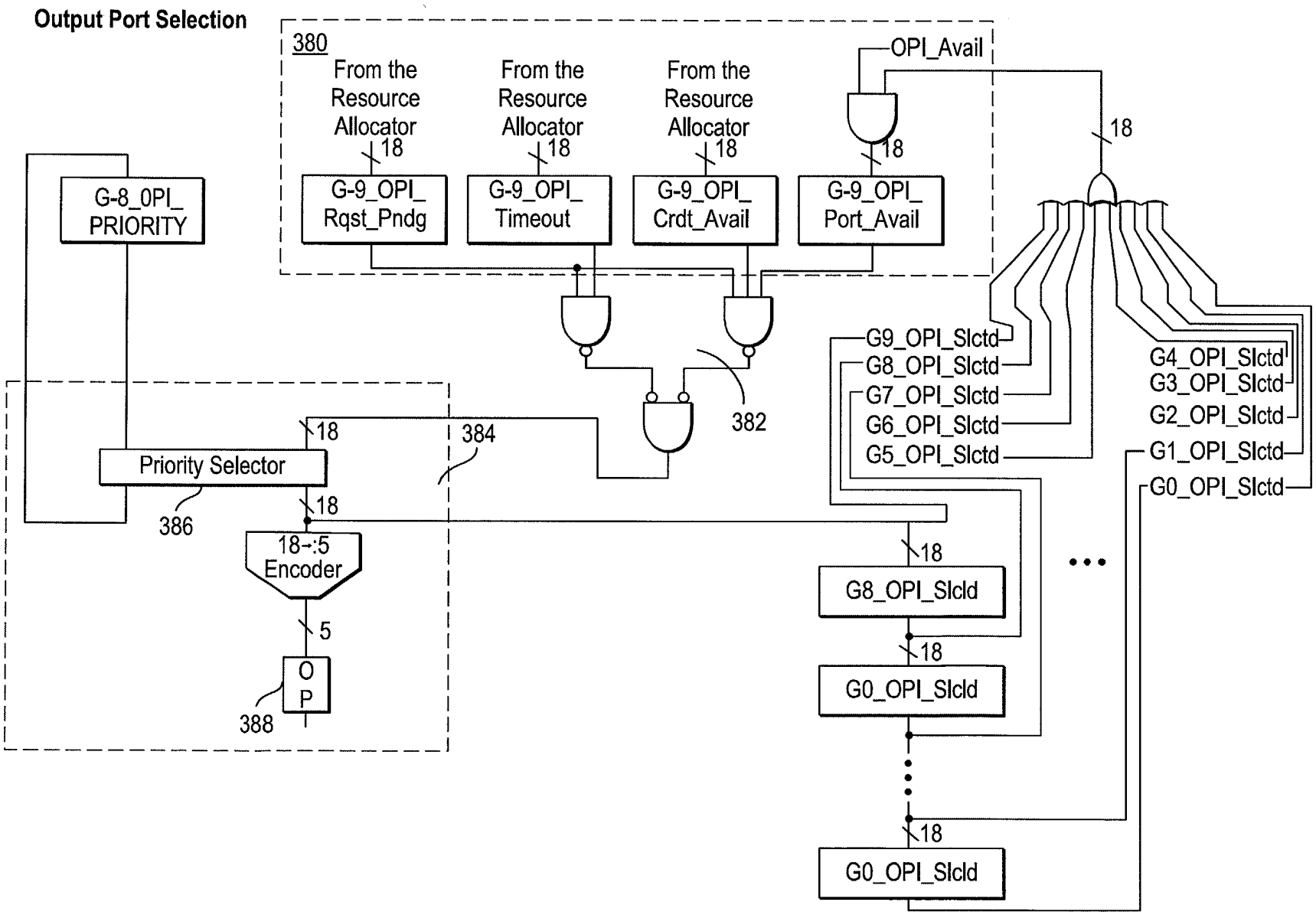

Output Port Selection
380
From the Resource Allocator
From the Resource Allocator
From the Resource Allocator
OPI_Avail
18
G-9_OPI_ Rqst_Pndg
G-9_OPI_ Timeout
G-9_OPI_ Crdt_Avail
G-9_OPI_ Port_Avail
G-8_0PI_ PRIORITY
382
384
Priority Selector
386
18-:5 Encoder
5
O P
388
G9_OPI_Slctd
G8_OPI_Slctd
G7_OPI_Slctd
G6_OPI_Slctd
G5_OPI_Slctd
G4_OPI_Slctd
G3_OPI_Slctd
G2_OPI_Slctd
G1_OPI_Slctd
G0_OPI_Slctd
G8_OPI_Slcld
G0_OPI_Slcld
G0_OPI_Slcld

Fig. 16A

Priority Management Table Read

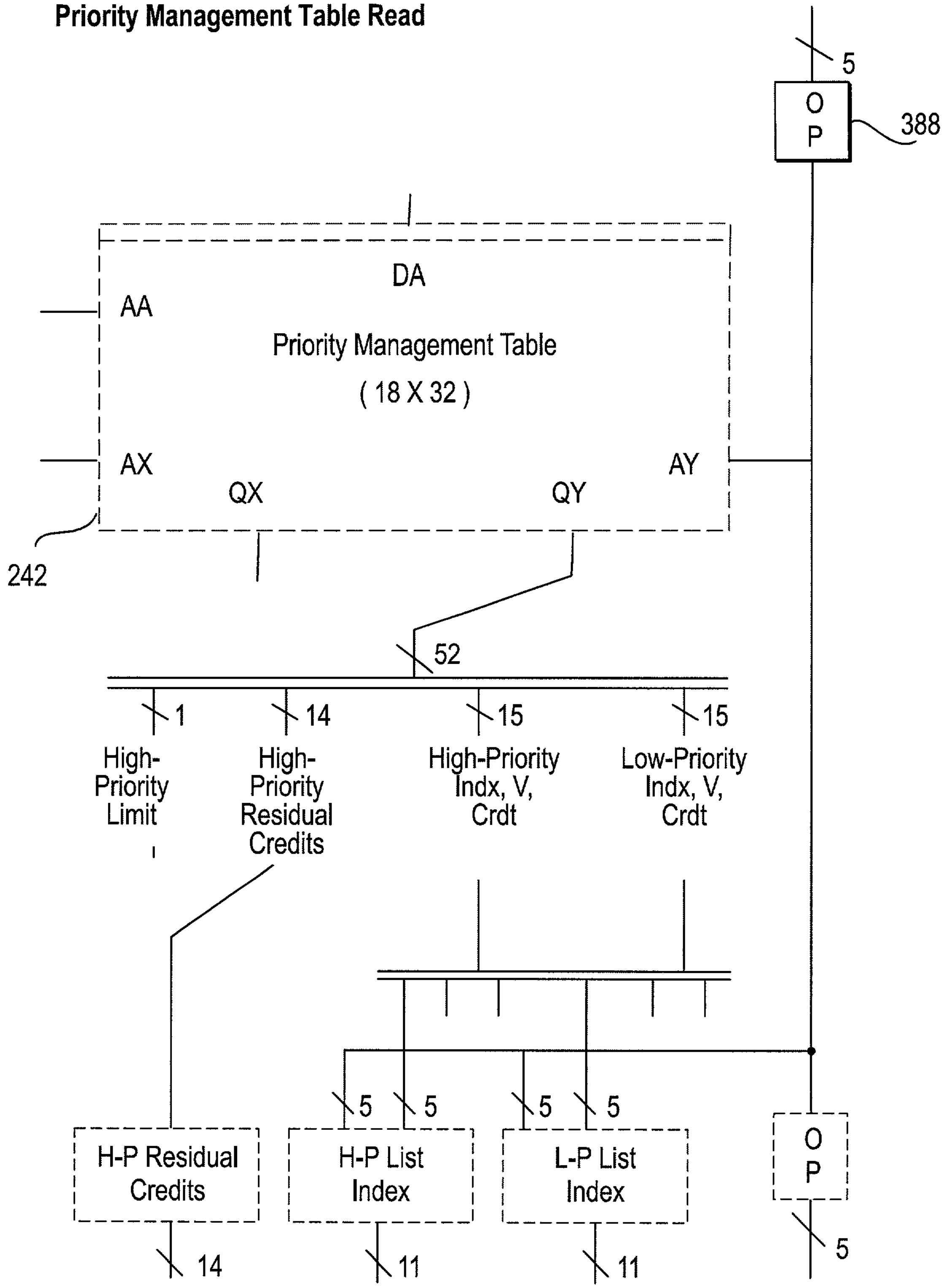


Fig. 16B

Virtual Lane Qualification

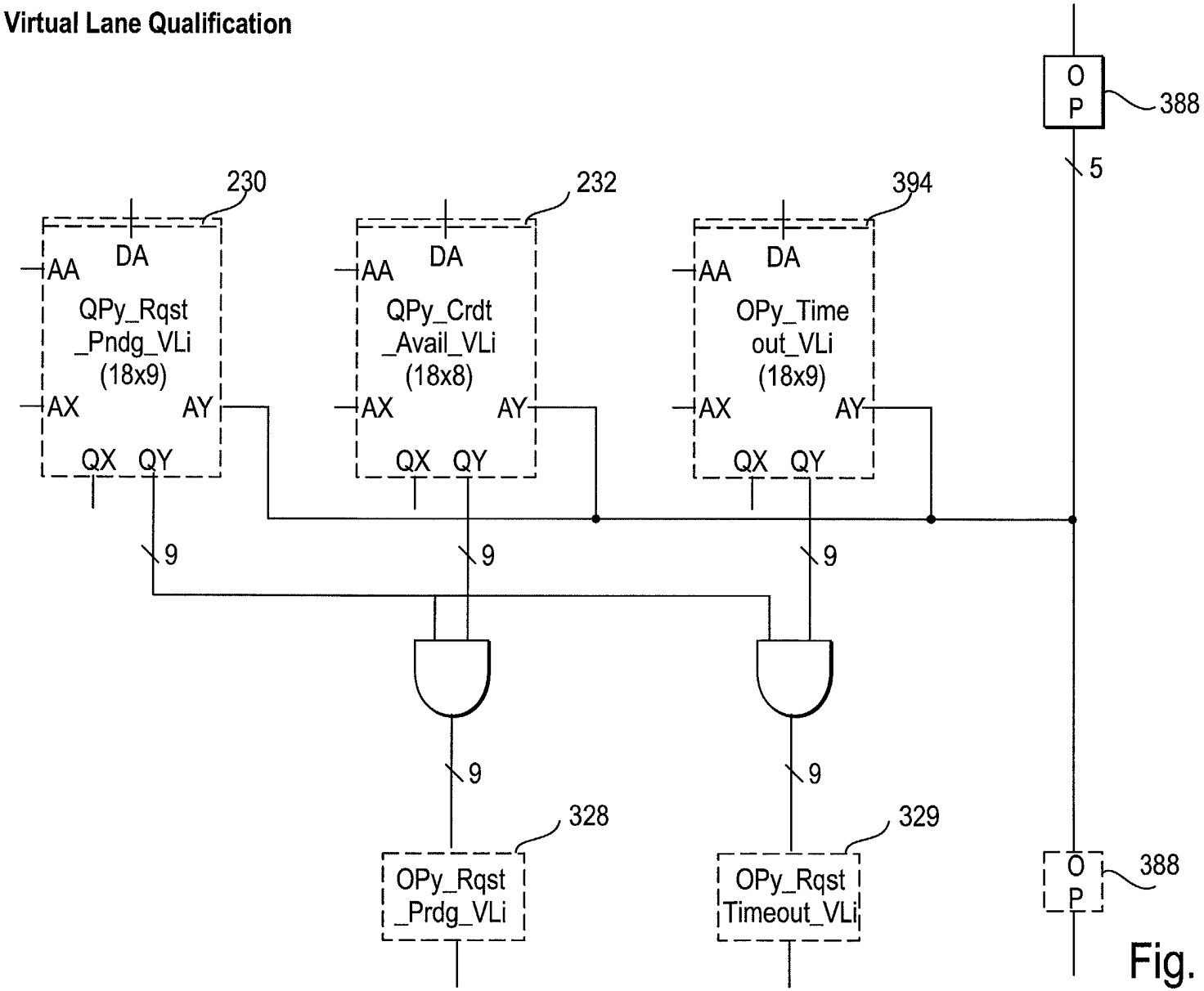


Fig. 16C

VL Priority Ranking Look-up

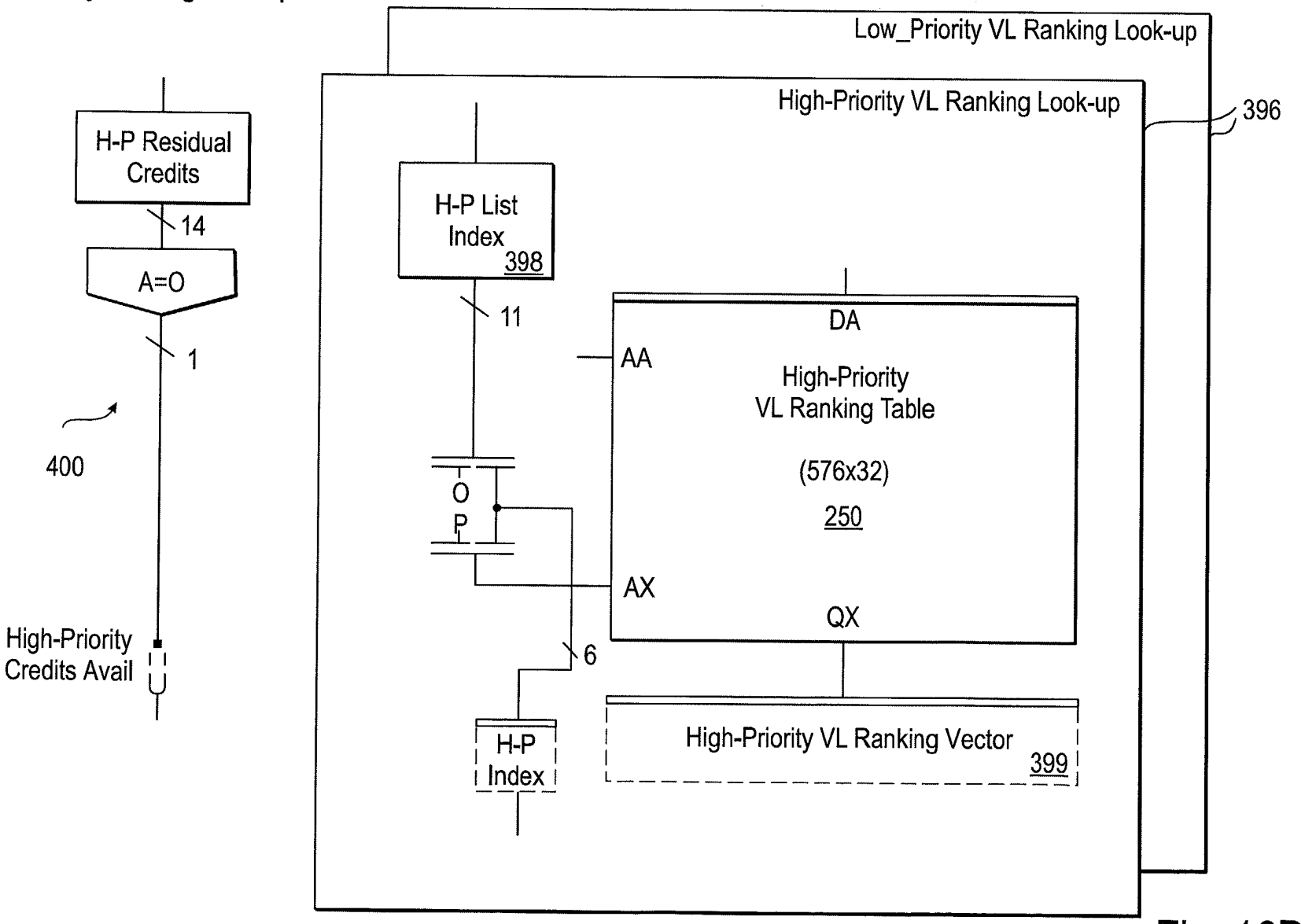


Fig. 16D

Virtual Lane Selection 1

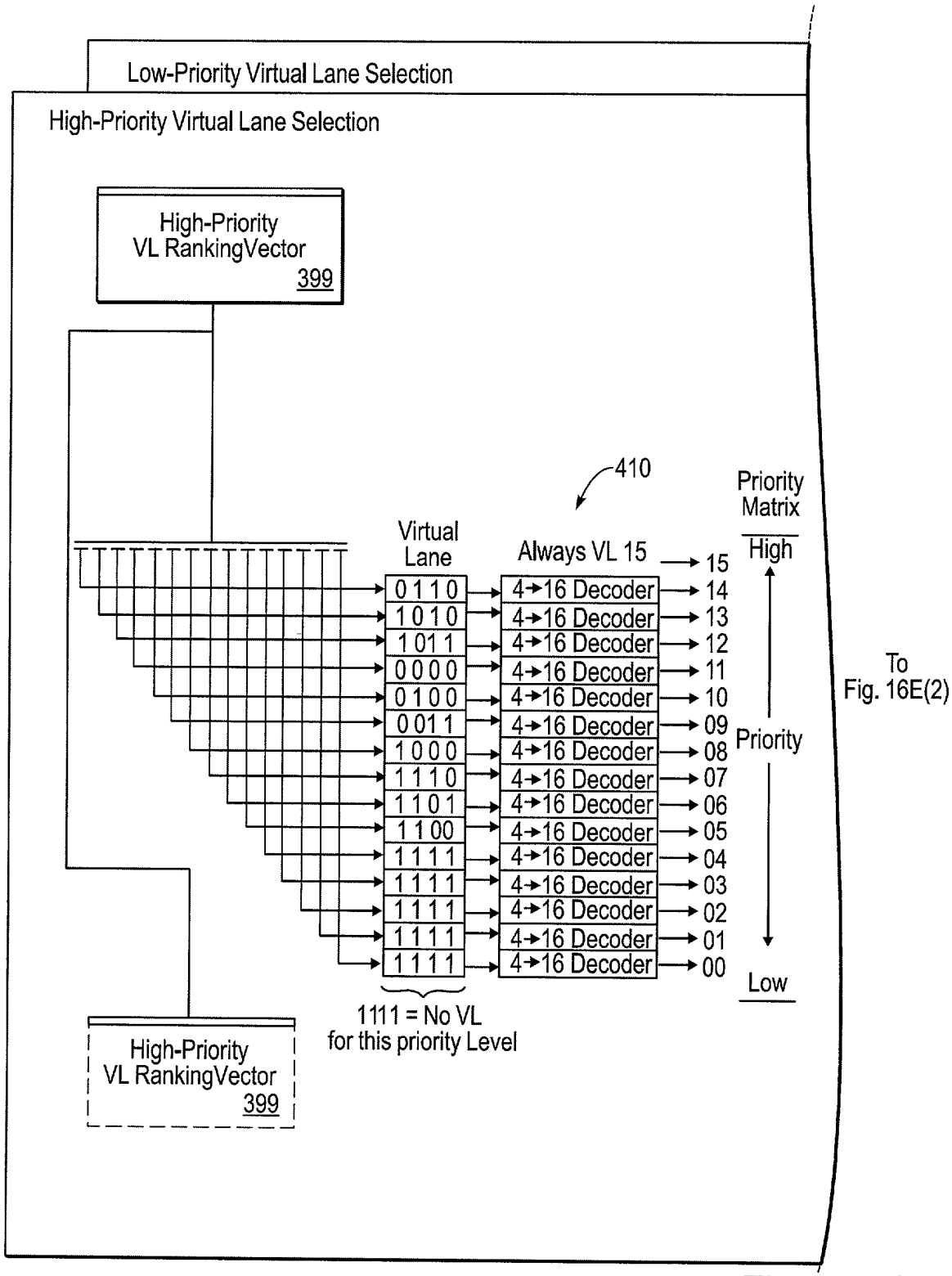


Fig. 16E(1)

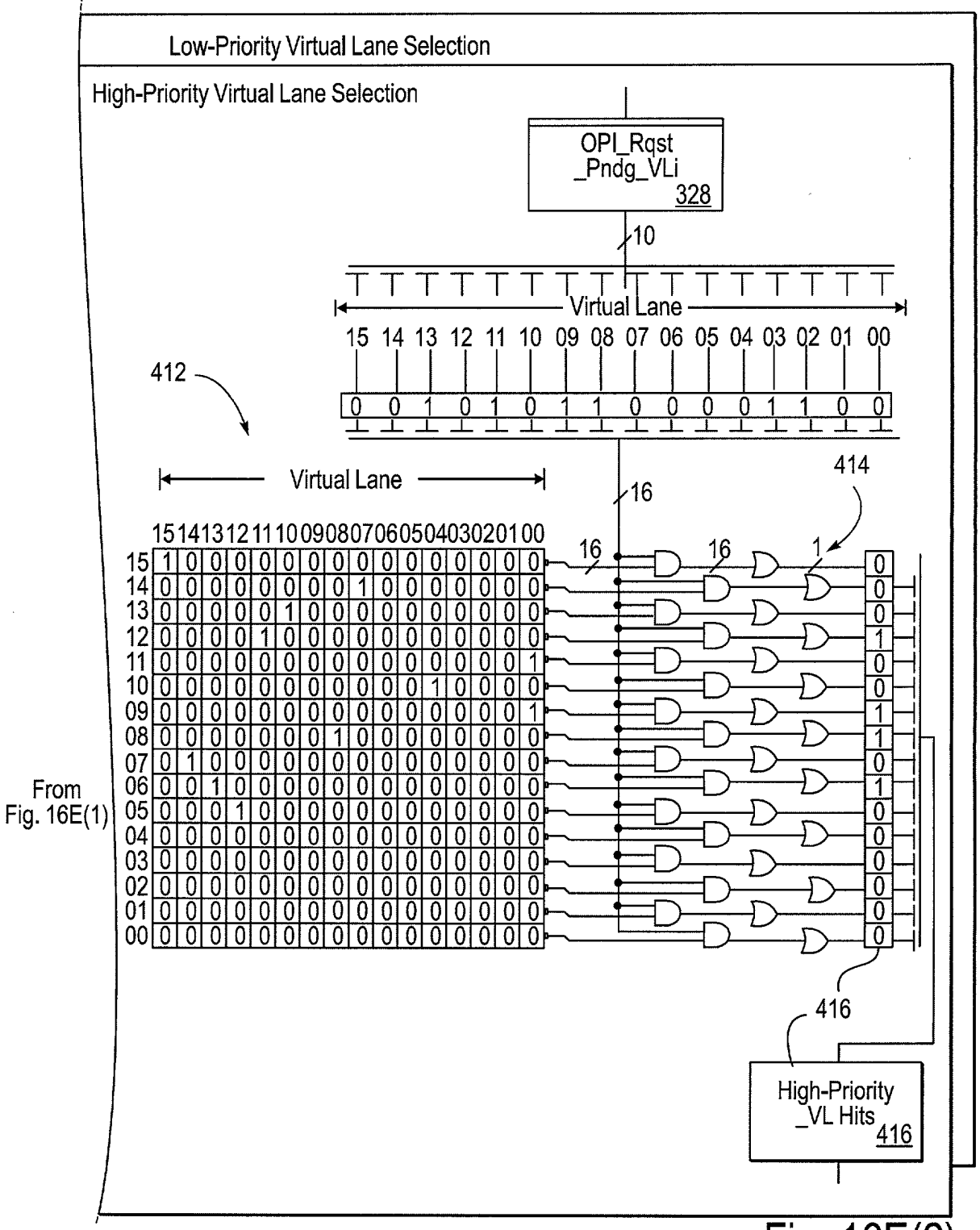

Low-Priority Virtual Lane Selection
High-Priority Virtual Lane Selection
OPI_Rqst
_Pndg_VLi
328
10
Virtual Lane
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
412
0 0 1 0 1 0 1 1 0 0 0 0 1 1 0 0
Virtual Lane
414
16
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
16
16
1
From
Fig. 16E(1)
416
High-Priority
_VL Hits
416

Fig. 16E(2)

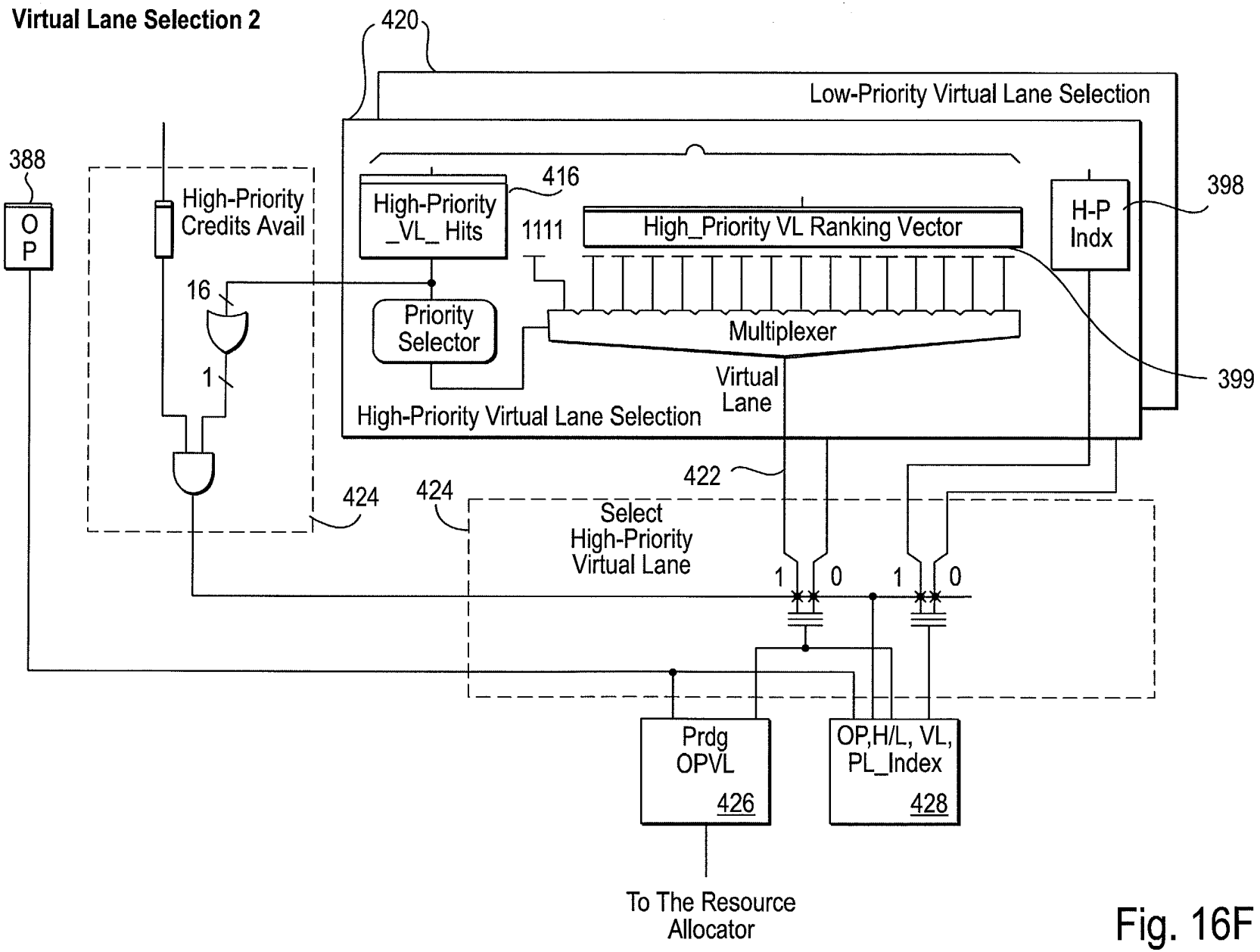

Virtual Lane Selection 2
420
Low-Priority Virtual Lane Selection
388
O
P
High-Priority
Credits Avail
16
1
High-Priority
_VL_ Hits
416
1111
High_Priority VL Ranking Vector
H-P
Indx
398
399
Priority
Selector
Multiplexer
Virtual
Lane
High-Priority Virtual Lane Selection
422
424
424
Select
High-Priority
Virtual Lane
1
0
1
0
Prdg
OPVL
426
OP,H/L, VL,
PL_Index
428
To The Resource
Allocator

Fig. 16F

Priority Map Lookup

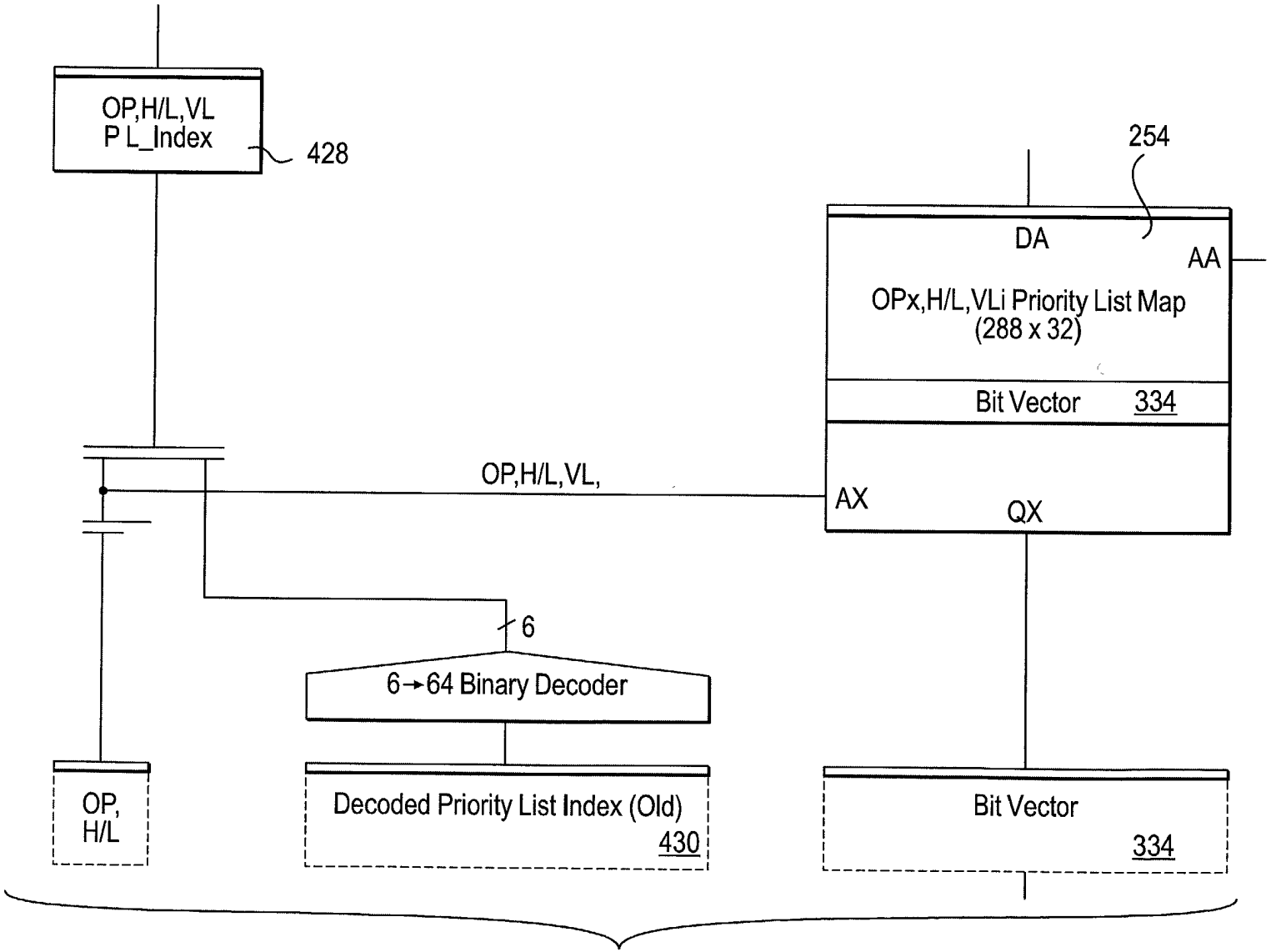


Fig. 16G

Priority List Index Computation

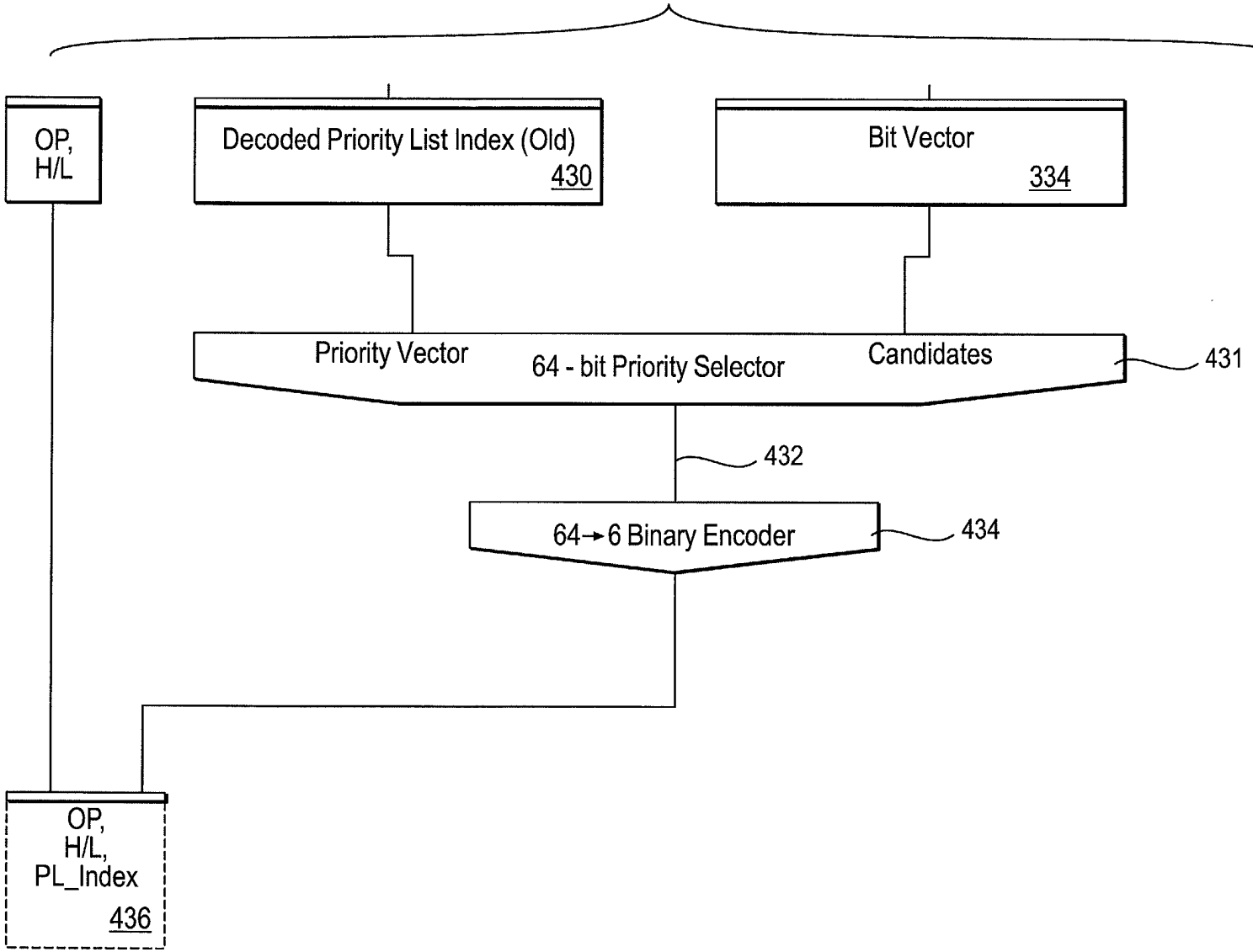


Fig. 16H

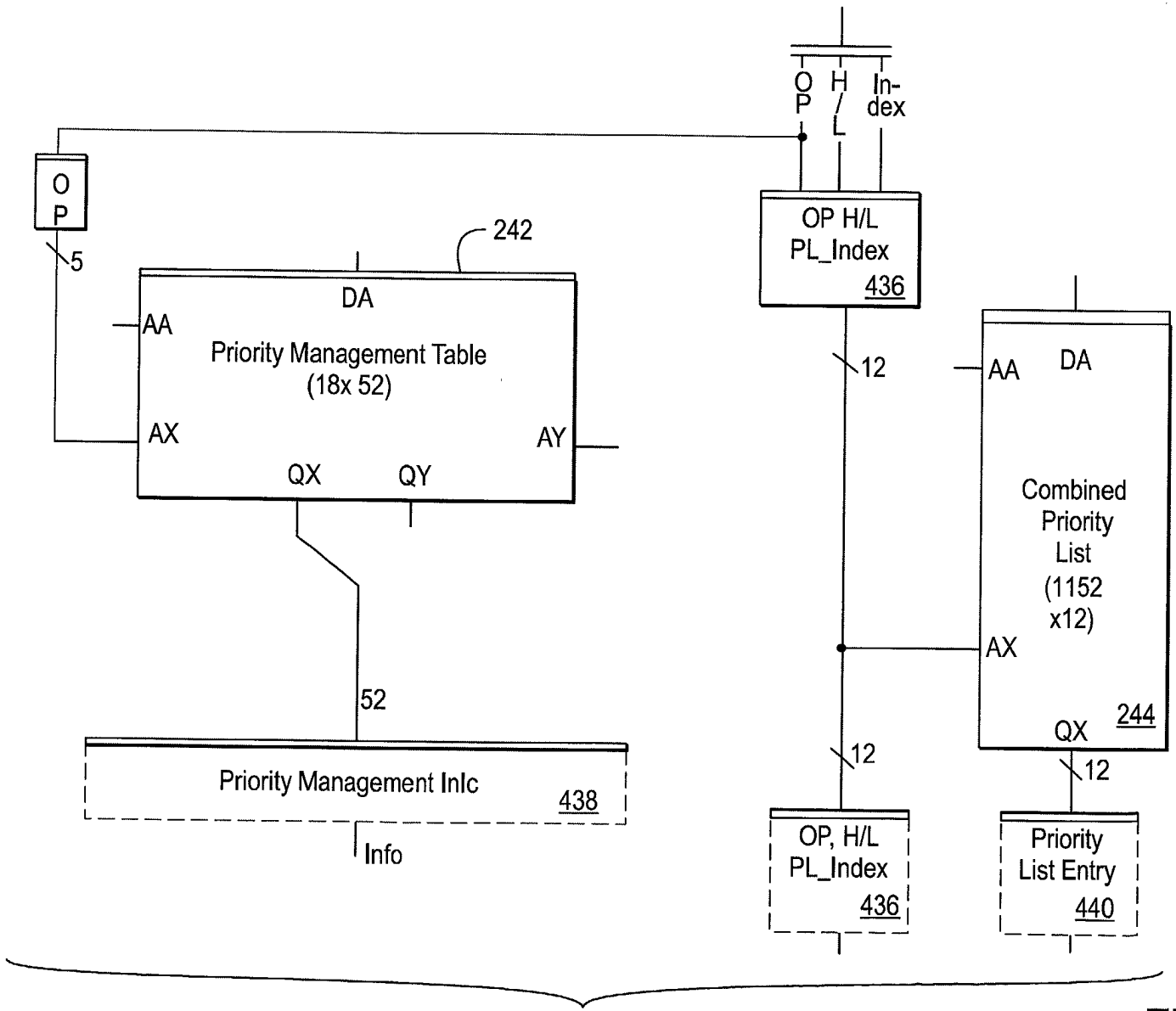

O P
H / L
In-dex
OP H/L PL_Index 436
O P
5
242
DA
AA
Priority Management Table (18x 52)
AX
AY
QX
QY
12
AA
DA
Combined Priority List (1152 x12)
AX
244
QX
12
52
12
Priority Management Inlc 438
Info
OP, H/L PL_Index 436
Priority List Entry 440

Fig. 16I

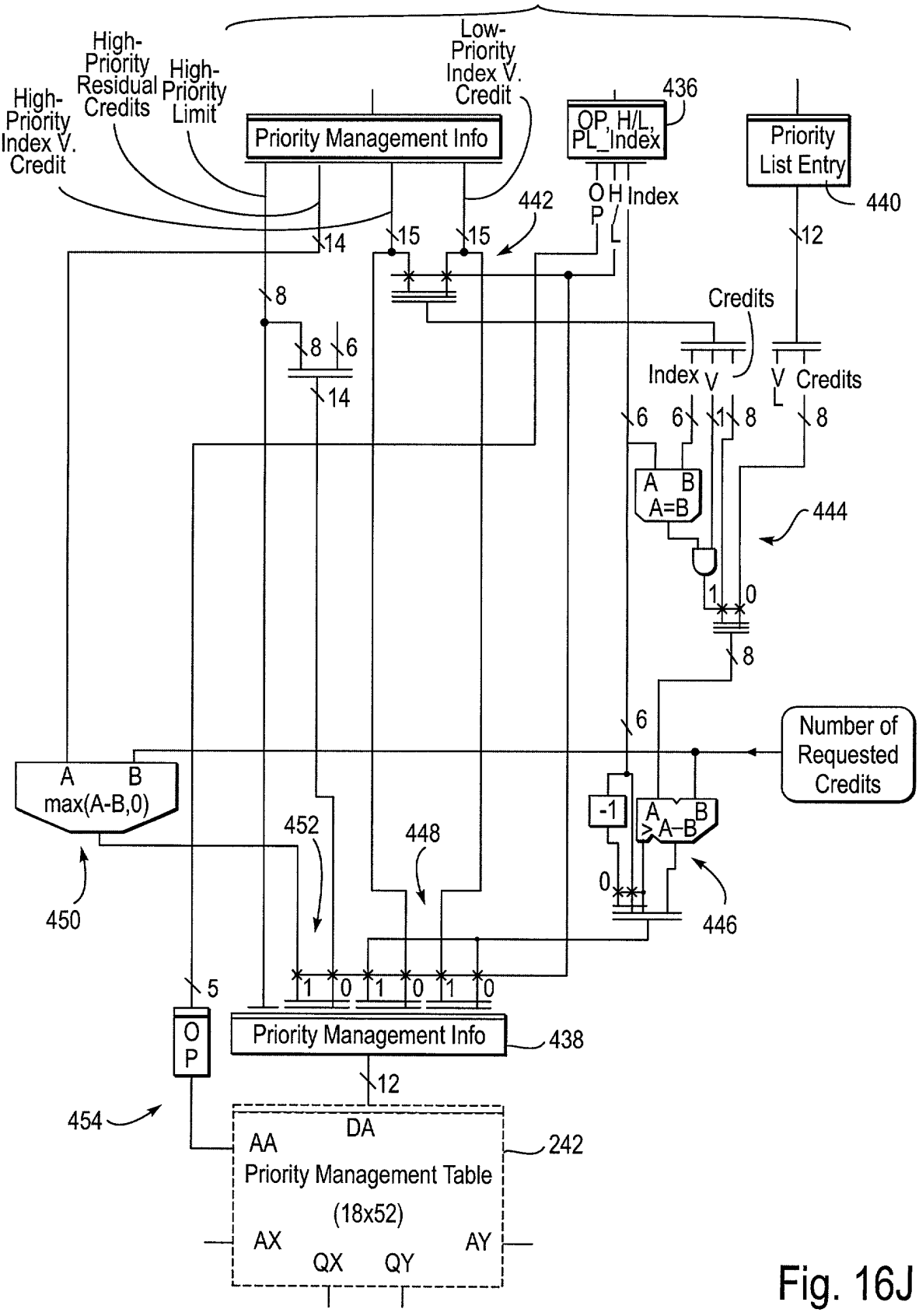

High-
Priority
Index V.
Credit
High-
Priority
Residual
Credits
High-
Priority
Limit
Low-
Priority
Index V.
Credit
Priority Management Info
436
OP, H/L,
PL_Index
Priority
List Entry
440
442
O
P
H
L
Index
14
15
15
12
8
8
6
14
Credits
Index
V
V
L
Credits
6
6
1
8
8
A
B
A=B
444
1
0
8
6
Number of
Requested
Credits
A
B
max(A-B,0)
450
452
448
-1
A
>
B
A–B
0
446
5
1
0
1
0
1
0
O
P
Priority Management Info
438
12
454
DA
AA
242
Priority Management Table
(18x52)
AX
AY
QX
QY

Fig. 16J

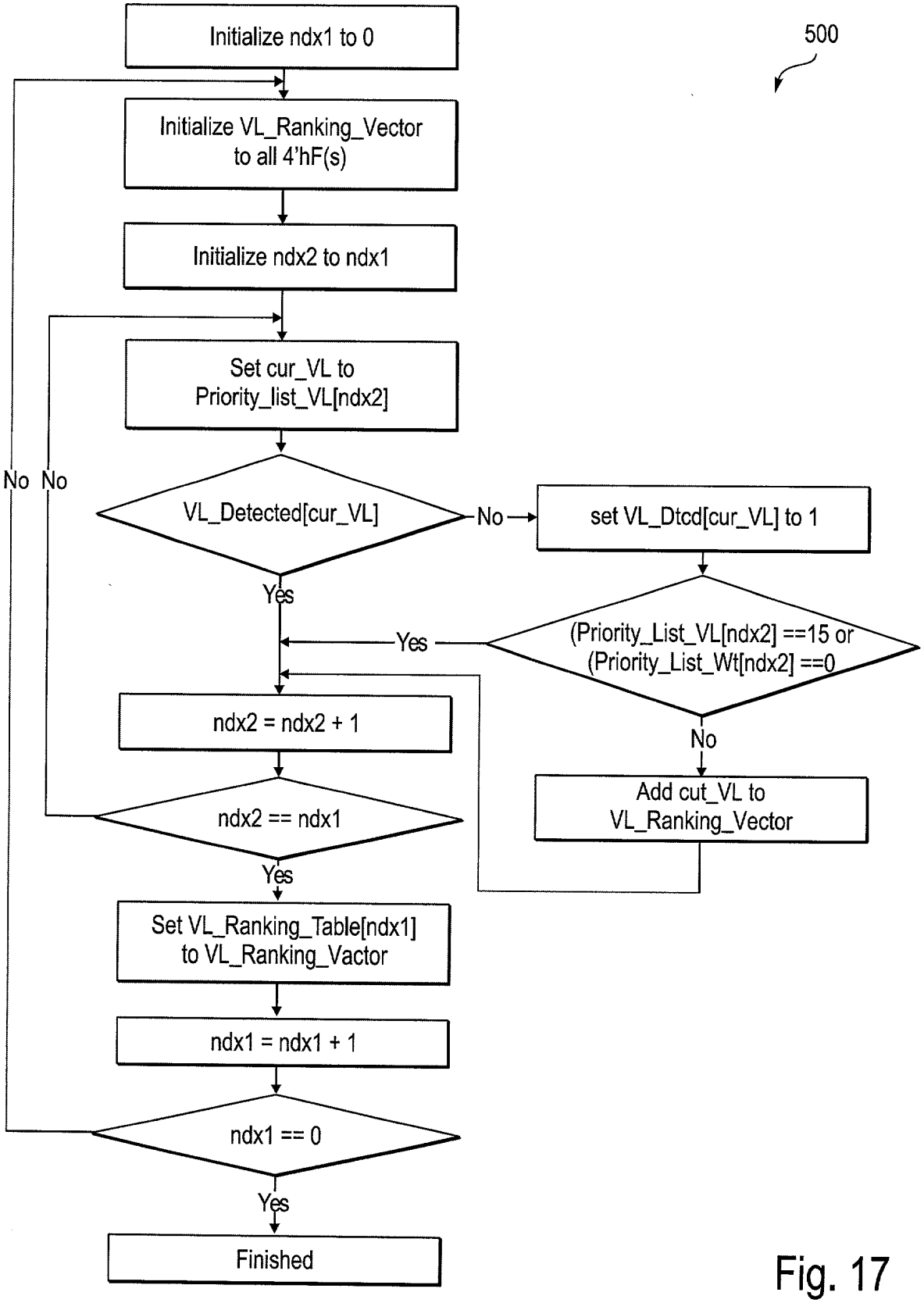

500
Initialize ndx1 to 0
Initialize VL_Ranking_Vector to all 4'hF(s)
Initialize ndx2 to ndx1
Set cur_VL to Priority_list_VL[ndx2]
VL_Detected[cur_VL]
No
set VL_Dtcd[cur_VL] to 1
Yes
(Priority_List_VL[ndx2] ==15 or (Priority_List_Wt[ndx2] ==0
Yes
No
Add cut_VL to VL_Ranking_Vector
ndx2 = ndx2 + 1
ndx2 == ndx1
No
Yes
Set VL_Ranking_Table[ndx1] to VL_Ranking_Vactor
ndx1 = ndx1 + 1
ndx1 == 0
No
Yes
Finished

Fig. 17

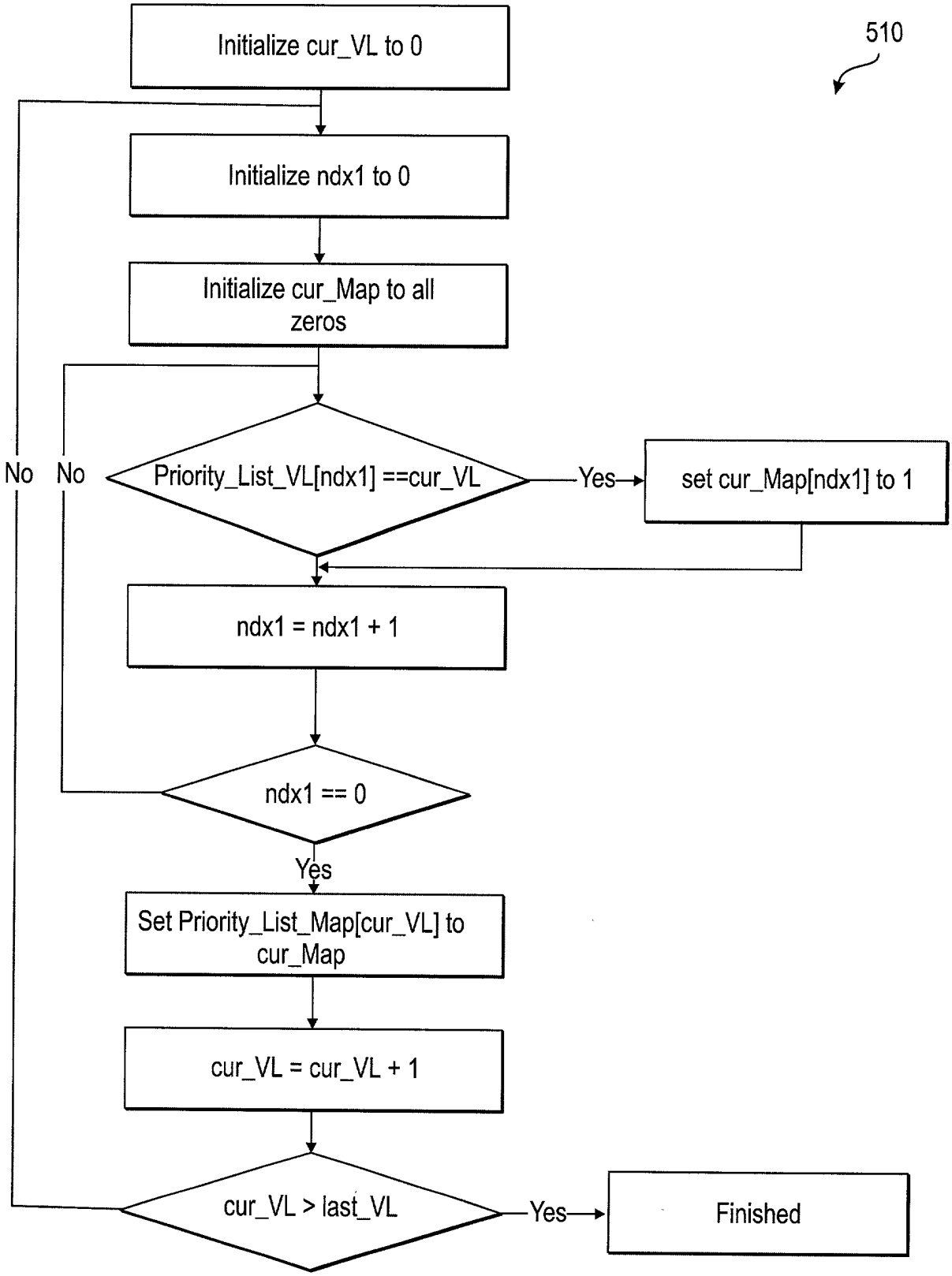

510
Initialize cur_VL to 0
Initialize ndx1 to 0
Initialize cur_Map to all zeros
Priority_List_VL[ndx1] ==cur_VL
Yes
set cur_Map[ndx1] to 1
No
No
ndx1 = ndx1 + 1
ndx1 == 0
Yes
Set Priority_List_Map[cur_VL] to cur_Map
cur_VL = cur_VL + 1
cur_VL > last_VL
Yes
Finished

Fig. 18